DC Polarity Control in Radio Frequency Synchronous Rectifier Circuits

Sheikh Nijam Ali, *Student Member, IEEE*, Thomas Johnson, *Member, IEEE*, and Deukhyoun Heo, *Senior Member, IEEE*

***Abstract*— In this letter, two different switching modes are identified for RF synchronous rectifier circuits which lead to a change in the polarity of the rectified output voltage. The operation of the two modes is defined in terms of the dynamic current–voltage (I–V) characteristics of the switching device and the polarity of the output load voltage. In one mode, the dc output voltage is positive and associated with a switching condition where the device is ON in quadrant-III and OFF in quadrant-I. This mode of operation has been reported widely in the literature. In the second mode, the quadrants associated with the on- and off-state are swapped leading to a polarity reversal across the load. Theoretical justification for the two modes is given and the experimental results are shown to confirm the two different switching modes in the synchronous rectifier. Experiments with a GaN inverse class-F rectifier were made to verify the theory, and both modes have similar measured peak rectification efficiencies of 77% at a frequency of 1.8 GHz.**

***Index Terms*— DC polarity control, GaN HEMT, high efficiency, inverse class-F, negative load voltage, RF power amplifier (PA), RF synchronous rectifier, time reversal duality, wireless charging, wireless energy harvesting, wireless power transfer.**

I. Introduction

RECENT work [1] has reported on how the principle of time reversal duality [2] can be used to convert efficient RF power amplifiers (PAs) into efficient synchronous rectifiers. The design methodology of time reversal duality has led to the development of many high-power RF synchronous rectifier circuits motivated by applications such as wireless power transfer, microwave power transmission from solar powered satellites, and wireless charging [3], [4].

In the literature reporting on the design of RF synchronous rectifiers, designs have solely focused on a switching condition that generates a positive load voltage. Under this condition, the switching device is OFF in quadrant-I and ON in quadrant-III. In this letter, we report on a second switching mode that reverses the ON- and OFF-state switching quadrants, which then leads to a negative output load voltage. The working principle of the negative polarity mode in the synchronous rectifier is described and compared with the positive polarity mode (conventional mode). Experimental results are presented to verify the theory of operation of the negative polarity mode using a GaN inverse class-F rectifier.

TABLE I
RELATIONS BETWEEN PA AND SYNCHRONOUS RECTIFIERS

Parameters	Positive polarity	**Negative polarity**
Drain-source voltage	$v_{RP}(t) = v_{PA}(-t)$	$\mathbf{v_{RN}(t) = -v_{PA}(-t)}$
Drain-source current	$i_{RP}(t) = -i_{PA}(-t)$	$\mathbf{i_{RN}(t) = i_{PA}(-t)}$
DC output power	$P_{DC,RP} = (V_{DC,PA})(-I_{DC,PA})$	$\mathbf{P_{DC,RN} = (-V_{DC,PA})(I_{DC,PA})}$
ON state	Quadrant-III	**Quadrant-I**
OFF state	Quadrant-I	**Quadrant-III**

II. Theory

Although the existence of different rectifier modes was theoretically proposed by Hamill [2], the implication of the different modes in terms of a practical switching devices and the experimental verification of different switching mode was not described.

The theory of time reversal duality rests on the reciprocity of power flow in a circuit [2]. In an amplifier, power flows from the dc supply and is converted to RF load power. In this way, the amplifier has the property of an inverter which converts dc to ac. In a synchronous rectifier, power flow is reversed and RF power is converted to dc load power [1]. As a rectifier, the dc supply node in the amplifier is converted to a dc source node, and the dc power flow is negative in terms of the amplifier dc port voltage and dc port current.

Power delivered by the rectifier dual can be obtained in two ways as summarized in Table I. In the positive polarity mode, the dc port has a positive voltage, and current is delivered out of the dc port to the load thereby reversing power flow with respect to the amplifier dual [i.e., $P_{\mathrm{dc,RP}} = (V_{\mathrm{dc,PA}})(-I_{\mathrm{dc,PA}})$]. In this way, the rectifier circuit is obtained from time reversing the voltage [i.e., $v_{\mathrm{RP}}(t) = v_{\mathrm{PA}}(-t)$] and time reversing the current with the addition of a change in the polarity of the current [i.e., $i_{\mathrm{RP}}(t) = -i_{\mathrm{PA}}(-t)$]. A second condition that leads to reverse power flow is to time reverse and change the polarity of the voltage waveforms [i.e., $v_{\mathrm{RN}}(t) = -v_{\mathrm{PA}}(-t)$] and only time reverse the current waveforms [i.e., $i_{\mathrm{RN}}(t) = i_{\mathrm{PA}}(-t)$]. In the latter case, this

Manuscript received May 01, 2017; revised August 09, 2017; accepted September 13, 2017. Date of publication October 10, 2017; date of current version December 4, 2017. This work was supported in part by the U.S. National Science Foundation under Grant CNS-1705026 and Grant CNS-1564014, in part by the Joint Center for Aerospace Technology Innovation, in part by the NSF Center for Design of Analog-Digital Integrated Circuits, and in part by the Natural Sciences and Engineering Research Council of Canada. *(Corresponding author: Deukhyoun Heo.)*

S. N. Ali and D. Heo are with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 USA (e-mail: nijam.rony@gmail.com; dheo@eecs.wsu.edu).

T. Johnson is with the School of Engineering, University of British Columbia, Kelowna, BC V1V 1V7, Canada (e-mail: thomas.johnson@ubc.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2017.2756850

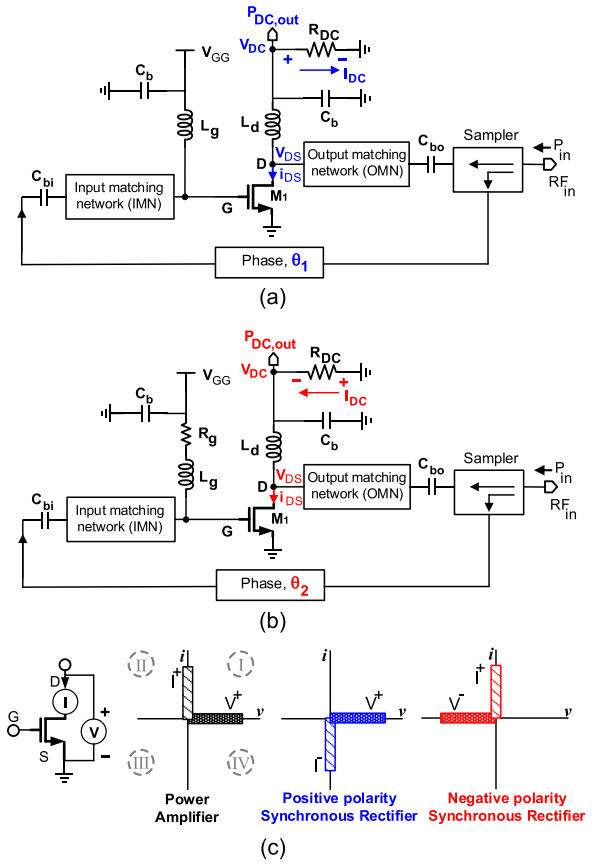

Fig. 1. Conceptual diagram of rectified dc current flow (I_{dc}) and voltage (V_{dc}) generation in a synchronous rectifier. (a) Positive polarity mode, (b) negative polarity mode, and (c) ideal device switching I–V characteristics for a PA and synchronous rectifiers with positive polarity and negative polarity.

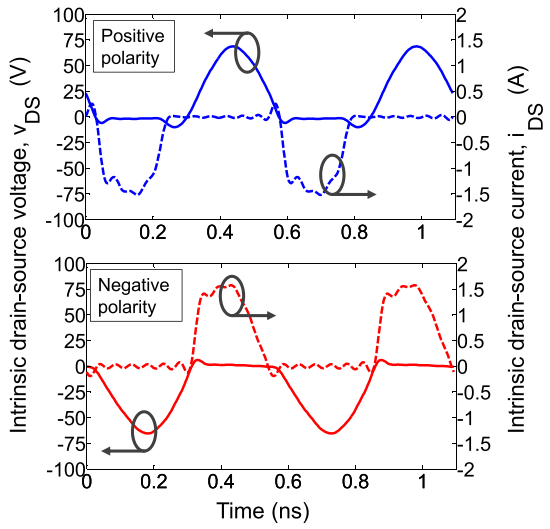

Fig. 2. Simulation results of intrinsic drain voltages (solid) and currents (dotted) of the realized inverse class-F synchronous rectifier at $P_{in} = 40$ dBm.

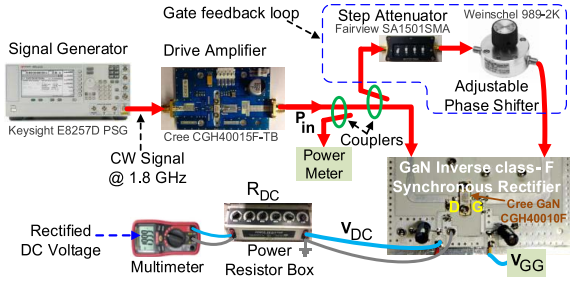

Fig. 3. Measurement test bench with an adjustable phase shifter in the gate feedback loop to control the rectified dc polarity.

leads to a negative load voltage with dc current flowing into the dc port terminal [i.e., $P_{dc,RN} = (-V_{dc,PA})\ (I_{dc,PA})$].

Although conditions that lead to negative power flow in time reversed amplifier circuits have been described [2], the link between device switching characteristics, dc load polarity, and phase in the gate feedback loop has not been described before. To continue further, we consider two examples of synchronous rectifiers which are shown in Fig. 1(a) and (b). In circuit (a), the load polarity is positive, while in circuit (b), the load polarity is negative. In both circuits, a transistor is used as the switching device and an appropriately phased gate drive signal is required to synchronously switch the device to generate waveforms that are the time reversed duals of the amplifier. The corresponding switching conditions with respect to the current–voltage (I–V) characteristics of the devices are shown in Fig. 1(c). In the positive polarity mode, the ON-state is in quadrant-III and the OFF-state is in quadrant-I, consistent with the condition that dc current flows out of the rectifier. In the negative polarity mode, the ON-state and OFF-state quadrants are reversed and load current flows into the rectifier generating a negative dc load voltage.

Further insight into the positive and negative load polarity, switching conditions are illustrated by the simulation results shown in Fig. 2. The simulation results are for a 1.8-GHz inverse class-F rectifier which uses a GaN-HEMT as the switch. With reference to Fig. 2, in the positive polarity mode, the drain voltage is positive with a half sine waveform, while the current is negative with a square wave shape. In the negative polarity configuration, the polarity of the voltage and current waveforms is reversed.

In self-synchronous rectifiers, the gate drive is derived from the RF input by a feedback loop, as shown in Fig. 1(a) and (b). Since the sign of the drain current has been reversed in the negative polarity mode compared to the positive polarity mode, the phase of the gate drive signal differs by 180° between the two polarities. In other words, $(\theta_2 - \theta_1) = 180°$ where θ_1 and θ_2 are the phase of the gate feedback loops shown in Fig. 1(a) and (b). The simulation results confirm that the two polarity modes can be obtained by adjusting the phase of the gate feedback circuit. Therefore, a reconfigurable feedback path which switches between two phase delays could be used to select the output polarity of the rectifier. This feature may be useful in various applications such as RF dc–dc converters [5]. We also note that although a gate bias is shown in the circuits of Fig. 1(a) and (b), other circuit topologies that can work with zero gate bias or self-generated bias may also be feasible depending on the device technology. For example, enhancement mode pHEMTs [3] and MOSFETs [6] have been used to implement other types of self-synchronous rectifiers.

III. Experimental Results

A 1.8-GHz inverse class-F synchronous rectifier was designed and implemented using a 10-W Cree GaN-HEMT

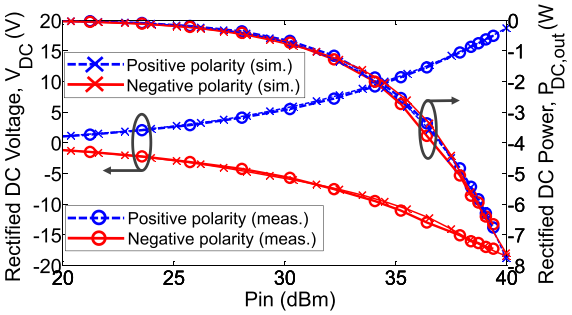

Fig. 4. Measurement and simulation results of rectified dc voltage and power for $R_{dc} = 45\ \Omega$, and gate bias condition of $V_{GG,RP} = -3.3$ V and $V_{GG,RN} = -5.2$ V.

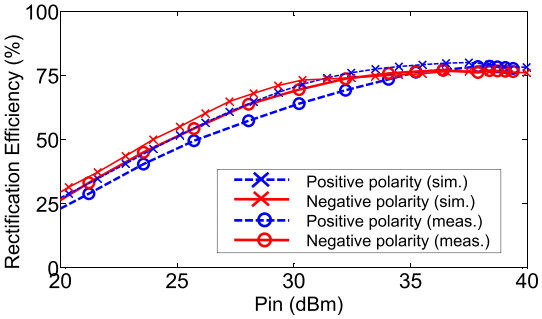

Fig. 5. Measurement and simulation results of rectification efficiency.

(CGH40010F) [7]. The output matching circuit had up to third-harmonic impedance control which is important to create orthogonal drain voltage and drain current waveforms that minimize overlap to obtain high efficiency. The gate drive feedback loop included an external phase shifter to control feedback phase. With the phase shifter, the same circuit could be configured to generate both positive and negative load voltages. Fig. 3 shows a photograph of the rectifier and the experimental test bench. The rectifier test bench consists of a RF signal generator with a drive amplifier from Cree (CGH40015F-TB). The additional amplifier was required to generate sufficient input power to test the rectifier. A power meter was used to calibrate the input power (P_{in}) to the rectifier. The external components in the gate feedback loop consist of a phase shifter and a step attenuator which were used to operate the rectifier in both polarity modes properly.

The detailed design and implementation of positive polarity inverse class-F synchronous rectifiers have been described before [7], but the implementation and operation of a negative polarity configuration are new. With reference to Fig. 1(b), the negative polarity circuit includes a series gate resistor R_g. This is essential to the circuit operation as a bootstrap mechanism is required to dynamically adjust the gate bias as the drain voltage peaks negative during the OFF-state. In this circuit, implemented with a depletion mode GaN-HEMT, the bootstrap is obtained by forward biasing the gate–drain junction and limiting gate current flow using R_g. For the experimental results shown here, the gate bias ($V_{GG,RN}$) for the negative polarity mode was -5.2 V, the gate resistance was 3.4 kΩ, and the forward bias gate current was 4.06 mA for a dc output voltage of -17.5 V. The gate bias current must be controlled to prevent damage to the device, and more robust circuit implementations of negative polarity circuits, perhaps with a diode shunting the gate and drain terminals, are recommended for future work.

Measurements were made to compare the performance of the rectifier under the two different polarity conditions. The dc load power ($P_{dc,out}$) and rectification efficiency were measured for a range of RF input power. A fixed dc load resistance (R_{dc}) of 45 Ω was found to maximize load power, and the polarity of the dc voltage was determined by the feedback phase shift. The difference in phase shift between positive load polarity and negative load polarity was measured to be 184°. The slight deviation from 180° is attributed to the device capacitances which modifies the phase inversion across the switch.

The measured dc load power, rectification efficiency [$(P_{dc,out}/P_{in}) \times 100\%$], and load voltage are plotted in Figs. 4 and 5. Simulation results are also shown for comparison with the experimental results. Good agreement between simulation and measurements results was obtained for both load polarity conditions. A peak rectification efficiency of 77% was measured for both rectifier polarities corresponding to a load voltage of approximately ± 17.5 V across a 45 Ω load. Measurements were taken over a 15-dB RF input range and both rectifier modes had similar performance with a rectification efficiency of greater than 40%.

IV. Conclusion

From the theory of time reversal duality, RF synchronous rectifiers can be designed to switch in two distinct ways which correspond to two different polarities in the output load voltage. Many experimental results demonstrating only the positive load voltage configuration have been published, and in this letter, new results are presented for a second switching mode which reverses the polarity of the load voltage. The negative load polarity mode reverses the ON- and OFF-state quadrants in the dynamic I–V switching plane. Experimental results show that the rectification efficiencies of both modes are approximately the same. Using these results, a dual polarity RF rectifier can be implemented by switching the phase in the gate feedback loop in self-synchronous designs. The dual polarity mode may have interesting applications in terms of RF dc–dc converters, wireless power transfer, and energy harvesting circuits.

References

[1] T. Reveyrand, I. Ramos, and Z. Popovic, "Time-reversal duality of high-efficiency RF power amplifiers," *Electron. Lett.*, vol. 48, no. 25, pp. 1607–1608, Dec. 2012.

[2] D. C. Hamill, "Time reversal duality and the synthesis of a double class E DC-DC converter," in *Proc. IEEE Power Electron. Spec. Conf.*, San Antonio, TX, USA, Jun. 1990, pp. 512–521.

[3] M. N. Ruiz, R. Marante, and J. A. García, "A class E synchronous rectifier based on an E-pHEMT device for wireless powering applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3.

[4] K. Huang and V. K. N. Lau, "Enabling wireless power transfer in cellular networks: Architecture, modeling and deployment," *IEEE Trans. Wireless Commun.*, vol. 13, no. 2, pp. 902–912, Feb. 2014.

[5] S. Djukic, D. Maksimovic, and Z. Popovic, "A planar 4.5-GHz DC-DC power converter," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 8, pp. 1457–1460, Aug. 1999.

[6] S. Dehghani and T. Johnson, "A 2.4-GHz CMOS class-E synchronous rectifier," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1655–1666, May 2016.

[7] S. Abbasian and T. Johnson, "Power-efficiency characteristics of class-F and inverse class-F synchronous rectifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4740–4751, Dec. 2016.