A Four-Element 500-MHz 40-mW 6-bit ADC-Enabled Time-Domain Spatial Signal Processor

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***Abstract*— Next-generation wireless communication requires phased-array systems with large modulated bandwidths and high energy efficiency, ensuring Gb/s data communication. Conventional phase-shifter-based arrays result in frequency-dependent processing and, therefore, beam-squinting in an array. This work demonstrates a four-element 500-MHz modulated bandwidth true-time-delay-based ADC-enabled spatial signal processor (SSP) with frequency-uniform beamforming, wideband beam-nulling, and multiple independent interference filterings using the Kronecker decomposition. This processor can augment conventional phased-array RF front ends to implement a complete antenna-to-digital solution. The proposed baseband delay-compensating solution in the SSP uses scalable time-domain circuits comprising of time-interleaved voltage-to-time converters followed by asynchronous 6-bit pipeline time-to-digital converters and consumes only 40 mW with a total area of 0.31 mm^2 in 65-nm CMOS technology.**

***Index Terms*— Kronecker decomposition, spatial signal processor (SSP), time-domain processing, true-time delay.**

I. Introduction

SPATIAL signal processing in multiantenna receivers offers not only higher received power and signal-to-noise ratio (SNR) because of a higher number of reception antennas but also enables spatial diversity and simultaneous communication with multiple devices. For the past several years, there have been many works on integrated multiantenna receivers. Approximating the time delay with a phase shift element is the basis of large portion of these works [1]–[8]. However, the frequency-dependent approximation of true-time-delay (TTD) with a phase-shift element results in beam-squinting in the angular domain [9] and limited fractional bandwidth (BW) in the frequency domain [10]. Using TTD with the spatial signal processor (SSP) results in frequency-uniform processing, which translates to beam-squinting free beamforming. The beam-squint issue has its parallel in beam-nulling arrays handling wide modulated bandwidths. The state-of-the-art phase-shifter-based arrays targeting beam-nulling [1], [4], [11]–[15] has limited rejection capability toward wideband interference because the array gain variation at different frequency components makes it hard to steer a deep null toward interference. For multiantenna receivers, it results in interference leakage and significantly higher dynamic range requirements for the baseband (BB) and the ADC [16].

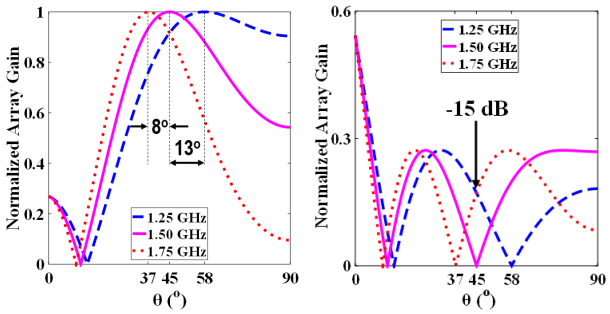

Fig. 1. Error due to phase shift in the angular domain over 500-MHz BW for (a) beamforming and (b) beam-nulling.

To emphasize the importance of the need for TTD SSP, a case study on the errors caused by phase-shift approximation in a linear array is presented. Assuming a four-element array with 500-MHz modulated bandwidth and 1.5-GHz center frequency, Fig. 1(a) shows that approximating TTD with a phase shifter results in $-8°$ and $+13°$ error in the angular domain (assuming angle of arrival (AoA) of 45° at the band edge). These errors are what are known as beam-squinting in a beamformer. Also, for beam-nulling, these errors result in limiting the filtering to only 15 dB, at the band edge. This can be observed in Fig. 1(b). The beam-squinting error further depends on the AoA. When the AoA increases, the beam-squinting gets worse. For high angles close to $\pm 60°$, the error at the band edges is as high as 28°. This results in non-alignment with the transmitter and consequently loss in the intended AoA.

Similarly, in the frequency domain, phase shifting results in frequency-dependent beamforming, which acts like a bandpass filter [see Fig. 2(a)] and affects the desired signal quality. Also, for the beam-nulling case, this approximation limits the rejection performance that, in this case, is only 15 dB at the band edges [see Fig. 2(b)]. This problem gets significantly more severe for larger arrays.

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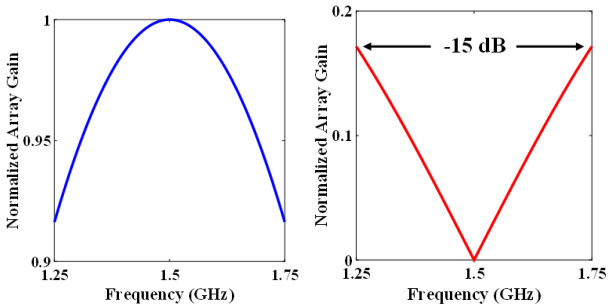


Fig. 2. Error due to phase shift in the frequency domain over 500-MHz BW for (a) beamforming and (b) beam-nulling.

TTD SSP can also be implemented in the digital domain, after digitizing all the channels [9]. This implementation gives complete access to the received signals at the cost of power-hungry ADCs. In contrast to prior approaches, our recent work [17] demonstrated a TTD SSP in the baseband (BB) time-domain prior to the ADC. In [17] and as shown in Fig. 3, we relaxed the data conversion resolution and, hence, power consumption requirement by filtering the high-power wideband blocker prior to the conversion, the TTD elements range and resolution requirements by implementing the TTD in the BB clock path [18], and all with digital-friendly time-based circuits and systems. This work significantly expands on the circuits and systems proposed in [17] with the following distinct contributions:

1) analysis of multiple independent interference cancellation in phased arrays using the properties of the Kronecker decomposition;
2) detailed circuit design of the SSP comprising voltage-to-time converter (VTC), time-to-digital converter (TDC), and time amplifier (TA) considering noise and linearity metrics;
3) expanded measurement methodology detailing the test setup and single-tone and wideband measurements for the SSP including the time-based ADC.

The rest of this article is organized as follows. Section II briefs SSP techniques in linear arrays for beamforming, beam-nulling, and independent cancellation of multiple interferences. The proposed system design and circuit implementation details are presented in Section III, combining discrete-time delay compensation with time-based ADCs. Section IV presents the measurement results for different SSP modes followed by conclusions in Section V.

II. SSP in Linear Arrays

Considering an N-element uniformly spaced linear array with half-wavelength spacing, the time delay between any two consecutive antennas can be represented as [19]

$$\tau = \frac{\mathrm{d}\cdot\sin(\theta)}{\mathrm{c}} = \left.\frac{\sin(\theta)}{2\cdot \mathrm{f_c}}\right|_{\mathrm{d}=\lambda_\mathrm{C}/2} \tag{1}$$

where λ_C and $\mathrm{f_C}$ are the received signal's wavelength and center frequency, respectively. These time delays between the received signals can be expressed in the frequency domain as an array vector, $\mathbf{V}(\mathrm{j}\omega)$, representing the antenna signals as a frequency domain vector

$$\begin{aligned}\mathbf{S}(\mathrm{j}\omega) &= L(j\omega)\cdot[1\ e^{-j\omega\tau}\ \ldots\ e^{-j\omega(N-1)\tau}]'\cdot X(j\omega)\\ &= L(j\omega)\cdot V(j\omega)\cdot X(j\omega)\end{aligned} \tag{2}$$

where $\mathbf{S}(\mathrm{j}\omega)$ is the received signals vector, scalar $\mathrm{L}(\mathrm{j}\omega)$ captures the path loss, and scalar $\mathrm{X}(\mathrm{j}\omega)$ is the transmitted signal. In the following, we will take advantage of this vector representation in the frequency domain to perform different spatial signal processing functions, including beamforming, beam-nulling, and independent cancellation of multiple interferences.

A. Beamforming

The time-delayed received signals at the antennas can be time-aligned first and then constructively combined to increase the power of the intended signal [10], [20]–[23]. This constructive addition is called beamforming, as shown in Fig. 4(a), and it can be also expressed in the frequency domain through the following vector expression:

$$\begin{aligned}\mathbf{Y}(\mathrm{j}\omega) &= [e^{-j\omega(N-1)\tau}\ e^{-j\omega(N-2)\tau}\ \cdots 1]'\cdot\mathbf{S}(j\omega)\\ &= N\cdot e^{-j\omega(N-1)\tau}\cdot X(j\omega)\end{aligned} \tag{3}$$

where $\mathbf{Y}(j\omega)$ is the beamforming output. As shown in (3), the amplitude of Y is higher than the X amplitude by a factor of N. This results in an improvement of N in the signal-to-noise ratio (SNR) as the signal power is increased by N^2 and the noise power is amplified only by factor of N.

The relation between the angle with the maximized received power and the implemented inter-element delay (τ) can be extracted from (1) and written as

$$\theta = \sin^{-1}(2f_C\cdot\tau). \tag{4}$$

Any deviation in the implemented inter-element time delay from the delay caused by the intended AoA results in drop in the beamforming gain. One form of deviation is the phase-shift approximation that neglects the frequency-dependency of the θ and causes non-uniform beamforming gain.

B. Beam-Nulling

Opposite to the beamforming, the received signals can be time-aligned and then destructively combined [18]. This destructive combination cancels the received signal and is called beam-nulling, as shown in Fig. 4(b). Similar to the beamforming case, beam-nulling can also be modeled in the frequency domain through vector representation

$$\mathbf{Z}(\mathrm{j}\omega) = [e^{-j\omega(N-1)\tau}\ -e^{-j\omega(N-2)\tau}\ \cdots -1]'\cdot\mathbf{S}(\mathrm{j}\omega) = 0. \tag{5}$$

The output of the beam-nulling system, $\mathbf{Z}(j\omega)$, is equal to zero, and the signal is nulled. In this spatial signal processing function, the undesired in-band interference can be filtered based on its AoA. To control the direction of the null, τ can be easily varied filtering the undesired signal from any direction.

Note that, in the beamforming case, there is a desired signal in which the receiver steers toward its direction and suppresses other directions. If there is a high-power interference located

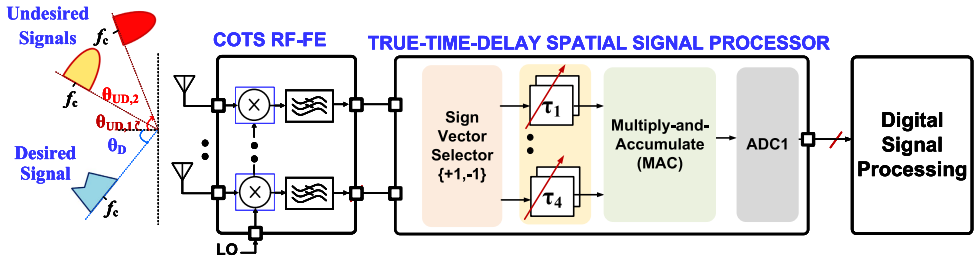


Fig. 3. Proposed BB delay-compensating TTD SSP. Only one beam is implemented.

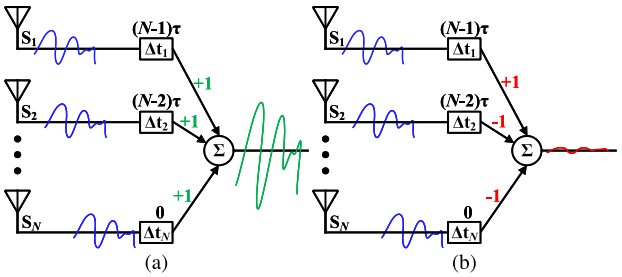


Fig. 4. TTD arrays for (a) beamforming and (b) beam-nulling.

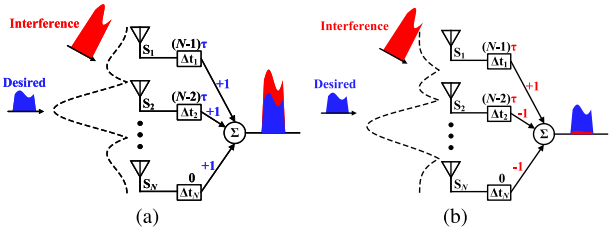


Fig. 5. (a) Beamforming of the desired signal results in high interference power at the output. (b) Beam-nulling the interference guarantees the immunity at the cost of lower desired gain.

in non-zero points of the beamforming gain (at the worst case, one of the sidelobes), the interference is not filtered enough and can potentially block the communication with the desired transmitter, as shown in Fig. 5(a). To solve this issue, the receiver can change to the beam-nulling mode to filter the high-power interference and receive the desired signal, as shown in Fig. 5(b). Note that the desired signal is affected by the beam-nulling conversion gain, depending on both the desired and undesired AoA. As mentioned earlier, the destructive combination (which is half of the channels being subtracted from the other half) in the beam-nulling implementation is chosen to maximize the desired signal gain. A limitation of the beam-nulling technique at BB is that the BB TTD implementation comes with the linearity overhead on the RF front end (RFFE), as the strong undesired signals must be down-converted without affecting the weak desired signal SNR.

C. Multiple Independent Interference Filtering

In Section II-B, a mathematical solution for filtering an interference with a specific AoA was presented. Even though that solution can offer multiple combinations for the interference cancellation, all the combinations null the same interference. This limitation makes a simultaneous multiple

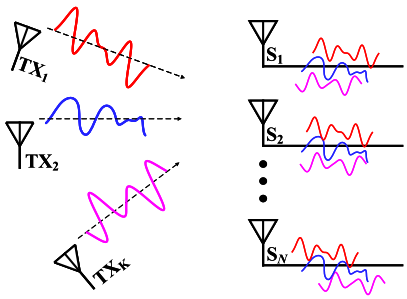


Fig. 6. TTD array cancelling multiple independent interferences.

independent interference cancellation solution attractive. In this section, a generalized approach to cancel multiple interferences in an N-element receiver is presented (see Fig. 6), where $K_{max} = \log_2(N)$ with K_{max} being the maximum number of transmitters.

Each transmitted signal is received at the receiver with its own unique array vector $(\mathbf{V_1}(j\omega), \ldots, \mathbf{V_i}(j\omega) \ldots, \mathbf{V_K}(j\omega)$, where $i = 1 \ldots, K$ and $K \leq K_{max}$. The constant τ makes the array vector entries to form a geometric sequence with scale factor of 1 and the common ratio of $e^{-j\omega\tau}$. This property offers a unique decomposition of the array vector through the Kronecker product of K_{max} sub-vectors [24] as follows:

$$\begin{aligned} V_i(j\omega) &= [1 \; e^{-j\omega\tau_i} \; \ldots \; e^{-j\omega(N-1)\tau_i}]' \\ &= [1 \; e^{-j\omega\tau_i}]' \bigotimes [1 \; e^{-j\omega 2\tau_i}]' \cdots \bigotimes [1 \; e^{-j\omega(N/2)\tau_i}]' \end{aligned} \tag{6}$$

where i is the array index, $N = 2^{K_{max}}$, and $\bigotimes$ denotes the left Kronecker product. In this operation, the entire first matrix is multiplied by each entry of the second matrix. Because any array vector $V_i(j\omega)$ can be decomposed into K_{max} 2×1 sub-vectors, there will be K_{max} 1×2 unique vectors that each null one of the decomposed 2×1 sub-vectors. The Kronecker product of any $1 \times (N/2)$ random vectors with the K_{max} 1×2 vectors can null the entire decomposed array vector. For example, the 1×2 vector that can null the first sub-vector of the first transmitter array in (6) is

$$\begin{aligned} &[e^{-j\omega\tau_1} \; -1] \bigotimes A(j\omega)[1 \; e^{-j\omega\tau_1} \; \ldots \; e^{-j\omega(N-1)\tau_1}]' \\ &= [e^{-j\omega\tau_1} \; -1][1 \; e^{-j\omega\tau_1}]' \bigotimes \widehat{A(j\omega)} \\ &= 0 \bigotimes \widehat{A(j\omega)} = 0 \end{aligned} \tag{7}$$

where $\widehat{A(j\omega)}$ is a new random vector and does not affect the outcome of the nulling. Similarly, the 1×2 vector that can

null the decomposed sub-vector of the second transmitter array can be expressed as

$$\begin{aligned}&[e^{-j\omega 2\tau_1} \ -1] \bigotimes B(j\omega)[1 \ e^{-j\omega\tau_1} \ \cdots \ e^{-j\omega(N-1)\tau_1}]' \\ &= [e^{-j\omega 2\tau_1} \ -1][1 \ e^{-j\omega 2\tau_1}]' \bigotimes \widehat{B(j\omega)} \\ &= 0 \bigotimes \widehat{B(j\omega)} = 0 \end{aligned} \quad (8)$$

where $\widehat{B(j\omega)}$ is a new random vector and does not affect the outcome of the nulling.

The final cancellation vector in this instance ($F_1(j\omega)$) for the $K = K_{\max}$ scenario can be written as

$$\begin{aligned}F_1(j\omega) = [e^{-j\omega\tau_1} \ -1] \bigotimes [e^{-j\omega 2\tau_2} \ -1] \\ \bigotimes \cdots [e^{-j\omega(N/2)\tau_{K_{\max}}} \ -1]. \end{aligned} \quad (9)$$

The subscript in $F_1(j\omega)$ shows the first possible solution, as there are $K_{\max}$ possible unique solutions depending on which order is chosen to null the sub-vectors (or which transmitter is called TX_1, TX_2, and so on). For the specific implementation with four elements, two independent interferences can be cancelled ($K_{\max} = \log_2 4 = 2$). The two possible solutions to cancel the interferences in this four-element receiver are as follows:

$$\begin{aligned}F_1(j\omega) &= [e^{-j\omega\tau_1} \ -1] \bigotimes [e^{-j\omega 2\tau_2} \ -1] \\ &= [e^{-j\omega(\tau_1+2\tau_2)} \ -e^{-j\omega(2\tau_2)} \ -e^{-j\omega\tau_1} \ 1] \end{aligned} \quad (10)$$

$$\begin{aligned}F_2(j\omega) &= [e^{-j\omega\tau_2} \ -1] \bigotimes [e^{-j\omega 2\tau_1} \ -1] \\ &= [e^{-j\omega(2\tau_1+\tau_2)} \ -e^{-j\omega(2\tau_1)} \ -e^{-j\omega\tau_2} \ 1]. \end{aligned} \quad (11)$$

Note that the outcome of (9) is a non-uniform delay implementation, in contrast with the constant inter-element delay implementation for the beamforming and beam-nulling cases. The beam-nulling and multiple independent interference cancellation performance can be further improved by implementing a real-time adaptive TTD control (for example, in [25]). In this delay optimization, the algorithm will find the best delay values to maximize the interference cancellation and, hence, the system SNR in contrast with a unique one-to-one mapping between the TTD element delay and the interference locations.

III. SSP System Design and Circuit Implementation

In Fig. 7, the system-level diagram of the designed four-element BB discrete-time time-domain SSP is presented. The proposed SSP is demonstrated with a 500-MHz modulated bandwidth, a sampling rate of 1 GS/s, and a 1-ns delay compensation range through two levels of time-interleaving, capable of beamforming, beam-nulling, and two independent interference cancellation modes. Similar to the charge-domain implementation in [10], the TTD elements are implemented through the BB delay compensation technique in the BB, accompanied by the LO phase-shifters. However, unlike the closed-loop OTA-based charge-domain implementation in [10], the signal combination in the time domain does not impose any extra bandwidth requirements. The TTD element in this design is implemented in the clock path through

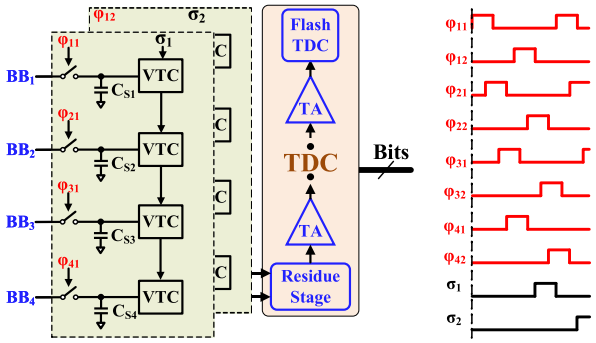


Fig. 7. Block diagram of the proposed four-element BB time-domain SSP with ADC.

a voltage-controlled delay line. This design's amplitude response purely depends on the capacitor and dc current mismatch, and the delay value does not affect the amplitude. In terms of amplitude correction/calibration, future research can implement a reconfigurable switched capacitor network instead of one single sampling capacitor or controlling the discharging current (of the voltage-to-time converter) similar to a current-starving digital-to-analog converter (DAC).

The proposed time-domain SSP is capable of three different processing modes. In Mode 1, the processor is in the beamforming mode, and all the BB signals are added constructively after time alignment through the delay compensating technique in the VTC sampling phase. By changing the processor sign vectors and time-aligning the interferences, half of the received signals are subtracted from the other half resulting in beam-nulling in Mode 2. Finally, in Mode 3, by taking advantage of the Kronecker decomposition of the array vectors, $\log_2(N)$ independent interferences can be filtered. The TTD elements in Mode 3 are not uniformly spaced (required inter-element delay is not constant for each pair of consecutive elements) and are calculated after the Kronecker decomposition. The sign vector and the required TTD elements for the four-element RX in Mode 3 can be found through (10) or (11).

In this implementation, the signal combination is performed in the time domain, where the first sampled BB input is converted to a time-domain pulse by the first VTC. By applying the output of the first VTC to the second one, the time-domain information of the second input, which is the time-domain representation of the second sampled value, is added (or subtracted) to the first one. This delayed version of CLK is then applied to the second VTC to generate a new delay proportional to the second sampled voltage. In other words, the sampled voltages of the first two inputs are combined and converted to a delay between the CLK and the output pulse of the second VTC. By continuing this trend for the remaining VTCs, all the input signals are added in the time domain at the output of the last VTC. The time-domain output of the last VTC, which contains all the sampled input information, is then digitized through an asynchronous pipeline TDC for further digital processing. At each stage of the TDC, two raw bits are extracted, and a residue value is generated and amplified by a TA, for the following stages.

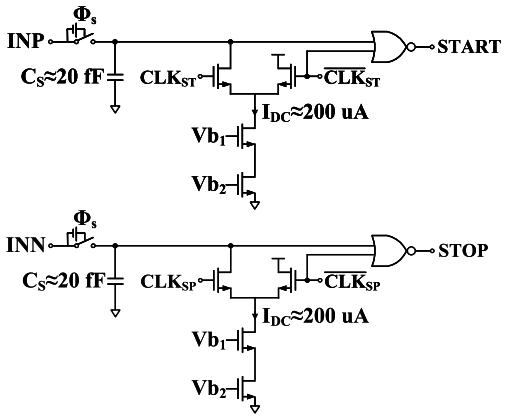


Fig. 8. Schematic of the differential VTC [17].

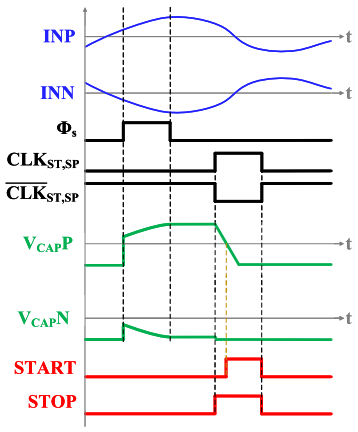


Fig. 9. Example of differential VTC operation.

In the end, all the bits extracted from different stages are combined in a specific timely manner to reconstruct the complete digital data. For TA calibration across the PVT variations, the particle swarm optimization (PSO) is used. The delay compensation values are generated through a tunable delay line explained later. Also, a 6-bit TDC is implemented to digitize the time-domain information for further processing. The TA linearity is enhanced by combining two different TAs with different input–output characteristics. The detailed implementation of each sub-blocks is presented next.

A. Discrete-Time VTC

A single-ended implementation of the VTC is shown in Fig. 8. In this VTC, the differential input continuous-time voltages (INP/INN) are sampled on the sampling capacitors ($C_S \approx 20$ fF), while the output pulses (START/STOP) are low. When the reference phases (CLK_{ST}/CLK_{SP}) rise, the capacitors are disconnected from the inputs and begin to discharge by the constant current $I_{DC}(= 200\ \mu A)$. Based on the sampled values on the capacitors, there will be T_{OUT} amount of time delay between the times that capacitors voltages cross the comparator reference voltage on each side. The comparator outputs (START/STOP) are triggered and rise when the crossing happens. This way, the continuous-time input voltage is first sampled and is then converted to a delay between START and STOP. The input–output characteristic of the VTC can be expressed as [26]

$$T_{OUT}[k] = \frac{C_s}{I_{DC}} V_{IN}[kT_S]. \tag{12}$$

From (12), the conversion gain of this VTC is equal to $C_s/I_{DC} = 100$ ps/V. The bootstrapped switch enhances the linearity and allows up to $1_{V_{pp,diff}}$ input voltage range while sampling at 1 GS/s. In the two time-interleaved VTCs corresponding to the first channel, the VTC reference clocks are connected to σ_1 and σ_2, respectively, and for the rest of the VTCs, they are connected to the previous VTC output pulses for signal combination.

The high-power interference signal in the cascaded VTCs causes the largest nonlinearities in the first stage (i.e., in the pair of VTCs connected to the first input), and this stage dominates the overall linearity as its nonlinearities propagate through the entire chain and will be present at the final time-domain value (i.e., the output of the last VTC). Any non-idealities in the first VTC can potentially get amplified by the following stages and reduce the overall performance. In this design, we have used the same VTCs for all the stages and tried to optimize the overall voltage to time conversion and not the individual stages.

An example of the VTC operation with non-overlapping sampling and reference phases is shown in Fig. 9. In the sampling phase, both the capacitors track the input voltage, while both the outputs are zero. By turning off the sampling switches, the capacitors hold the sampled value, while the outputs are still low. When the reference phase arrives, if the sampled value on the capacitor (V_{CAPP} or V_{CAPN}) is less than the NOR gate threshold voltage, the corresponding output, STOP (corresponding to V_{CAPN}), in this example, rises, while the other output remains low. V_{CAPP} begins to discharge by the constant current source, the moment V_{CAPP} reaches the NOR gate threshold voltage, and the corresponding output, START, rises. Thus, the continuous-time input voltages are sampled and then converted to two pulses that the delay between them is proportional to the difference between the sampled values. The falling edge of the reference clocks synchronizes the output falling edges. Thus, the delay between the rising events is only of interest.

B. Asynchronous Pipeline Time-to-Digital Converter

To quantize the time-domain spatially processed output of the VTCs, an asynchronous pipeline TDC, with four residue stages, four TAs each with a gain of two, and a 2-bit flash TDC is implemented, as shown in Fig. 10. The input time-domain pulses are first applied to the first residue stage, where two raw bits with the most significant bit (MSB) value are extracted and a residue value is generated. The residue value is first amplified through a TA and then applied to the second residue stage. This trend continues until the fourth (last) residue stage where the output residue value is amplified and then quantized through the 2-bit flash TDC. Besides the bits and the residue value, at each stage, an asynchronous pulse (VALID) is generated for

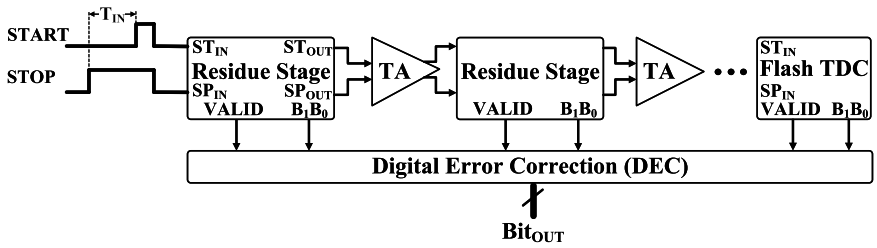


Fig. 10. Block diagram of the proposed asynchronous pipeline TDC.

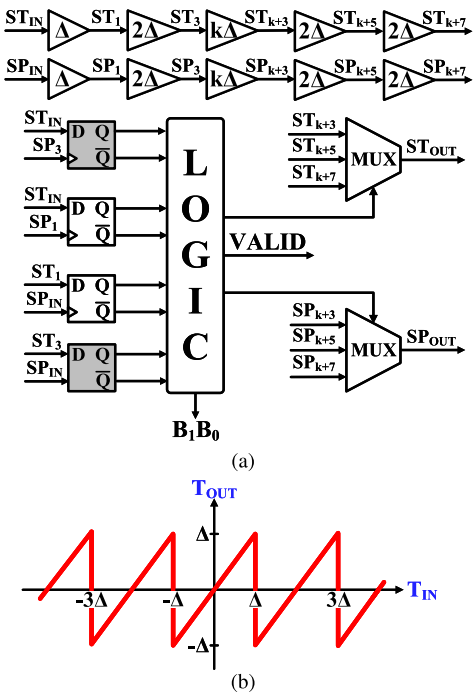


Fig. 11. (a) Proposed 1.5-bit residue stage. (b) Transfer characteristics of residue stage.

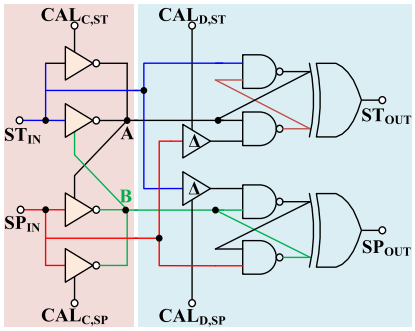


Fig. 12. Block diagram of companding-expanding TA.

proper timing of the raw bits combination in the digital error correction (DEC) block.

The residue generation is implemented by a 1.5-bit residue stage, as shown in Fig. 11(a). In this implementation, the operation region is detected by comparing the different delayed versions of the input pulses (ST_{IN} and SP_{IN}) through a time-domain comparator, which is an arbiter that detects early or late arrival of one input compared with the other one. The delayed version of the input pulses is generated through a delay line with an inter-stage delay of $\Delta = 40$ ps. Based on the arbiter outputs, the LOGIC unit determines the operation region and generates the raw bits. After the region detection and the bit extraction, the LOGIC also generates the asynchronous VALID pulse as the operation validation. The VALID pulse is the outcome of the case that all the arbiters have settled to their final result. The residue generation, which, basically, is the controlled shift in the input time value (T_{IN}), is performed by selecting the different delayed version of input pulses as the output (ST_{OUT} and SP_{OUT}). Compared with the conventional pipeline residue stage, two extra time comparators (highlighted in gray) are added to limit the output residue value range. The input–output characteristic of the designed 1.5-bit residue stage with the extra time comparators is shown in Fig. 11(b). By removing the extra comparators, the output residue range can get as high as $\pm 3\Delta$, and this directly affects the TA linearity. Because the TA linearity is the main bottleneck in this design, adding two extra time comparators is well justified with minimal power penalty. The output residue value then is amplified by a factor of two and applied to the following residue stage.

As the output range of the first residue stage is $\pm\Delta$, the second residue stage input range is limited to $\pm 2\Delta$, and hence, the extra comparators will not be needed in the second residue stage. This range limitation applies to the third and fourth residue stages as well. Therefore, two extra time comparators are only needed in the first residue stage.

As mentioned earlier, the TA linearity determines the overall TDC linearity and, consequently, its signal-to-noise-distortion-ratio (SNDR). To enhance the TA linearity, two TAs with different input–output characteristic are combined. The block diagram of the combined TA with a gain of two is shown in Fig. 12. In this implementation, two sub-TAs (blue and red parts of Fig. 12) are combined to increase the overall time amplification linearity. The companding sub-TA [27] is based on multipath discharging shown in Fig. 13(a). In this technique, both the inputs are inverted through two inversion paths, where one of the paths is enabled by the inverted version of the other input. For instance, in Fig. 12, inverted version of ST_{IN} (node A) enables or disables one of the discharging paths of the other input (SP_{IN}) and, consequently, varies the delay from SP_{IN} to node B. This variation in the discharging power results in time amplification with a gain of approximately two. This approximation is mostly valid for small values of input but for larger input values the gain begins to drop.

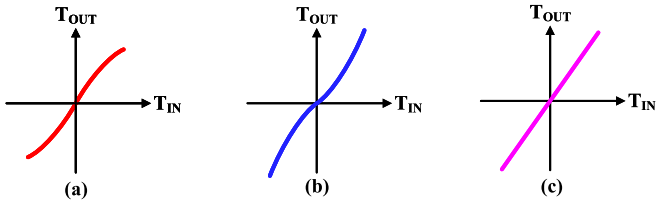


Fig. 13. Transfer characteristic of (a) companding sub-TA, (b) expanding sub-TA, and (c) proposed combined TA.

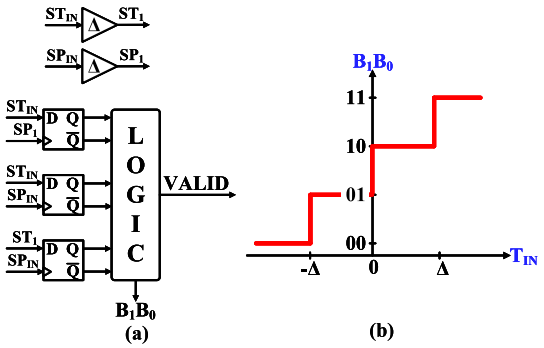


Fig. 14. (a) 2-bit flash TDC with (b) transfer characteristic.

On the other hand, the metastability-based expanding sub-TA that is implemented through cross-coupled NAND gates [28] results in an expanding characteristic, as shown in Fig. 13(b). By combining these two different characteristics, the TA linearity is enhanced, as shown in Fig. 13(c), and consequently, the TDC SNDR is improved. For both the sub-TAs, calibration nodes are included to maintain the required SNDR with the PVT variations. The PSO is used to calibrate the TA. This optimization is explained with the presented measurement results in Section IV.

The 2-bit flash TDC block diagram and the input–output characteristics are shown in Fig. 14. Similar to the residue stage, the output bits of the flash TDC are found by comparing different delayed versions of the input pulses. The pipeline nature of the implemented TDC requires a careful bit combination, performed in a timely manner. The found raw bits of the residue stages of the flash TDC are stored in D flip-flops clocked with the VALID pulse from each stage. After time alignment of the raw bits, they are added with 1-bit redundancy to ensure the proper pipeline quantization, similar to the conventional pipeline voltage-domain ADCs.

IV. Test Setup and Measurement Results

The presented BB TTD SSP is fabricated in a 65-nm TSMC process as a proof of concept. The die micrograph and the test setup for the SSP are shown in Fig. 15. The chip occupies 0.82 mm^2 area with only 0.31-mm^2 active core area. To validate the prototype, various measurements have been performed using a Quad-Flat No (QFN) Leads packaging. All the input signals are MATLAB generated and then uploaded to a Xilinx ZCU111 Evaluation Board. The signals are applied to the device under test (DUT) after dc biasing using bias tees. The reference 1-GHz clock is provided off-chip from an HP8664A signal generator. Through this reference clock, the required

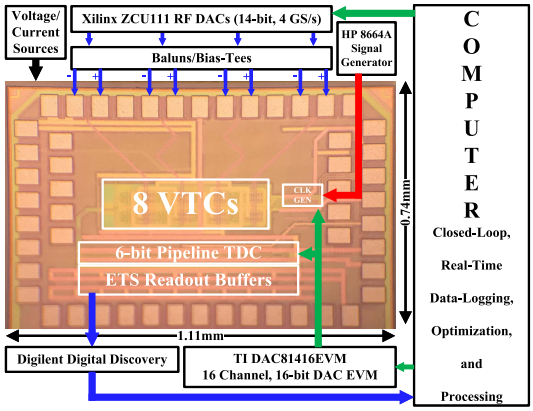


Fig. 15. Die micrograph and the test setup used for the TTD SSP.

time-interleaved phases for sampling are generated on-chip. The implemented inter-element delays are controlled externally through a 16-bit Texas Instruments (TI) DAC Evaluation Module (DAC81416EVM). The TI DAC is also used to tune the TA calibration nodes. Finally, the output digital data is read at a lower speed (40-MHz clock rate, 25× lower than the ADC operation speed) through a Digilent Digital Discovery board. To reconstruct the original data from the low-speed read-out, an equivalent time sampling (ETS) technique has been used followed by post-processing in MATLAB. The ETS read-out technique is commonly used in digital sampling oscilloscopes, where the input data are sampled at a lower rate, stored in the memory, and displayed later after the original data reconstruction [29].

Each channel's input-to-output characteristic is measured by applying a constant amplitude signal to each input (one at a time) and observing the digital output amplitude. The gain mismatch between the channels is initially calibrated by equalizing each input amplitude. After the channel mismatch calibration, the TDC and, specifically, the TAs are calibrated through PSO in the closed loop. The PSO is performed one time before the normal operation of the chip. In the PSO, 400 particles are used, representing 400 possible solutions for the TA calibration node voltage values. A single-tone input is applied to the chip, and the TDC SNDR is measured and stored for all the 400 possible solutions. Based on the outcome SNDR of each of the 400 particles for one iteration, the location of the particles that result in lower SNDR values is changed toward the particles with higher corresponding SNDR values in the next iteration. This trend is continued for 12 iterations until all the particles are close enough to the maximum possible value for the SNDR of the TDC. The SNDR value of all the particles versus the optimization iteration is plotted in Fig. 16, where, after each iteration, the particles are getting closer and closer to the maximum possible SNDR. The SNDR enhancement through the PSO can be seen in Fig. 17, where, for both cases of low frequency and Nyquist input, SNDR increases by more than 6.4 dB through this optimization.

The implemented SSP has been tested for the three processing modes and various types of input, including single-tone, wideband, and modulated signals. We have assumed that the RF-FE is operating at the 1.5-GHz center

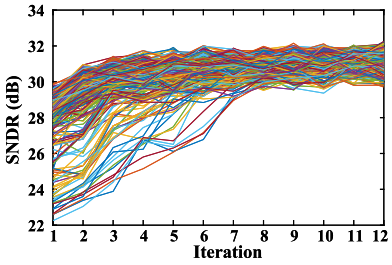


Fig. 16. TDC SNDR of each particle plotted versus the iteration index.

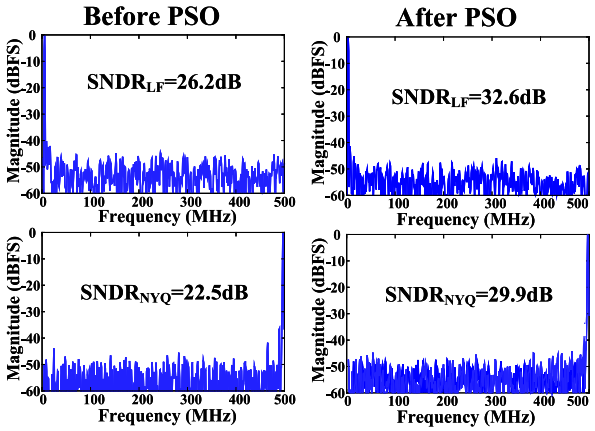
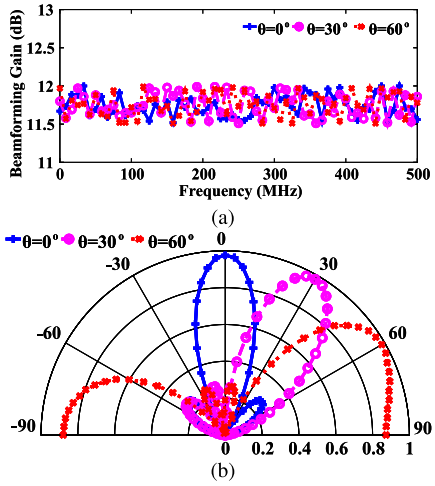


Fig. 17. TDC linearity enhancement through the PSO.

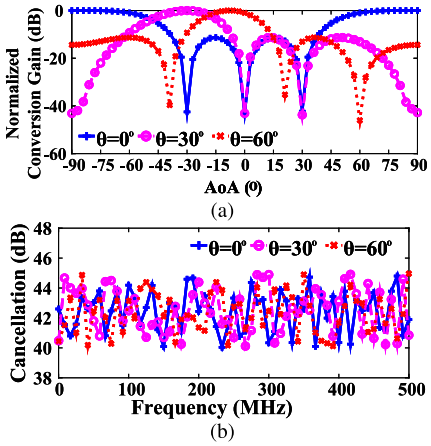


(a)

(b)

Fig. 18. Measured single-tone test results in the beamforming mode. (a) Conversion gain versus input signal frequency. (b) Beam patterns for the three different AoAs.

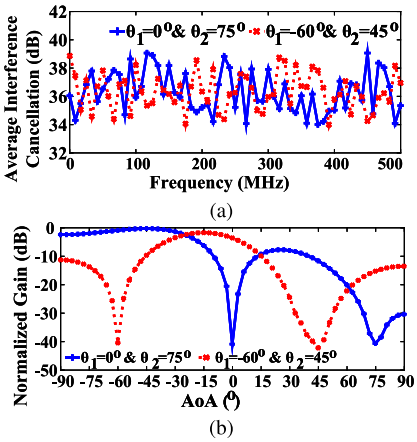
frequency, with antenna spacing of $\lambda/2$ (10 cm) and $\pm 90°$ angle coverages. These numbers result in a maximum inter-element delay of 1 ns/3 and the overall delay range of 1 ns. In Fig. 18(a), the measurement result of the chip in the beamforming mode and for a swept single-tone input signal is presented. For three cases of desired AoA, (0°, 30°, and 60°), frequency-independent beamforming gain of close to 12 dB is measured across the 500-MHz bandwidth. The jitter in the sampling phases and limited TDC resolution are the main reasons for the small variation in the beamforming



(a)

(b)

Fig. 19. Measured result of the single-tone test in the beam-nulling mode. (a) Conversion gain versus input signal frequency. (b) Cancellation for three AoAs.



(a)

(b)

Fig. 20. Measured single-tone test in Mode 3. (a) Average cancellation versus frequency. (b) Angular response for two pairs of interference AoA.

gain. For the three cases of AoA, the beamforming beam patterns of the processor are presented in Fig. 18(b). The frequency-independent beamforming conversion gain and the beam-squinting free beam patterns show the TTD-based operation of the SSP.

The same single-tone test is performed for the beam-nulling conversion gain versus the input signal frequency, and the beam-nulling patterns of the TTD SSP for three different interference AoAs are presented in Fig. 19(a) and (b), respectively. More than 40-dB interference cancellation is observed for the time-domain SSP across the entire bandwidth, in the beam-nulling mode. Also, deep angular nulls are generated in the beam pattern, providing high-performance beam-nulling.

The time-domain design is also validated for the two independent interference cancellation modes, where two undesired input signals with different AoAs are applied to the chip, and the processor filters both the undesired signals. In Fig. 20(a), the average cancellation of the undesired signals is plotted versus their single-tone frequencies, for two different pairs of interference AoA. On average, more than 34-dB cancellation is measured in Mode 3, proving the high-performance capability of the implemented design. The angular domain response of

TABLE I
PERFORMANCE OF THE PROPOSED TIME-DOMAIN SSP AND COMPARISON TO THE PRIOR ART

		[1] JSSC 2017	[4] JSSC 2019	[9] JSSC 2019	[18] TMTT20	This Work
Architecture		Phased-shift array	Phased-shift array	Digital TTD array	TTD array	TTD array
Implementation		RF + BB	mmWave + BB	RF + BB + DIG	BB	BB
# Elements		4 inputs / 4 outputs	4 inputs / 4 outputs	16 inputs / 16 output (4 beams)	4 inputs / 3 outputs	4 inputs / 1 output
Functionality		Arbitrary Spatial Filtering	Beamformer + Multi-Blocker Rejection	Beamformer + ADC	SpICa	Beamformer + Multi-Blocker Rejection + ADC
Domain		Voltage	Voltage	Voltage	Charge	Time
Technology		65nm CMOS	45nm SOI	40nm CMOS	65nm CMOS	65nm CMOS
Supply (V)		1.2	NR	NR	1.0	1.0
# Elements (N)		4	4	16	4	4
Rejection (dB)	Single-Tone	51-56	50-62	47	46-51	40-46
	Modulated BW	NR	28.5[1]	NA	>35	24
Rejection Mod. BW (MHz)		CW	500[2]	NA	100	500
Beamforming Mod. BW (MHz)		NR	500[2]	100	-	500
TTD Range (ns)		NA	NA	7.5	15	1
Operational Frequency Range (GHz)		0.1-3.1	27-41	0.95-1.05	0-0.1	1.25-1.75
Fractional BW (Mod. BW /RF Carrier Frequency)		NR	1.8% (0.5GHz/28GHz)	10.0% (0.1GHz/1GHz)	100.0% (0.1GHz/0.1GHz)[3]	33.3% (0.5GHz/1.5GHz)[3]
Linearity	P_{1dB} (dBm)	NR	-27.3 (Canc. OFF)	NR	4.7[4,5]	-0.5 (Canc. OFF)[4,5]
	IP3 (dBm)	-29[6,7]	-15[7,8]	NR	10.6[4,5]	7.9[4,5]
Noise Performance		3.4-5.8 dB Noise Figure	4.3-6.3 dB Noise Figure	60 dB SNDR	330 μV_{rms} (Output-referred)	32.6 dB SNDR
Power (mW)		116-147[9]	280-340[9]	453	52	25 (8 VTCs) 12 (TDC) 3 (Clock) 40 (Total)
Area (mm^2)		2.25[9] 1.44 (active)	23.4[9]	4.42 0.29 (active)	0.9	0.82 0.31 (active)

NR: Not reported; NA: Not applicable; [1]SINR in presence of two 256-QAM 100M Sym/s blockers; [2]Raw bandwidth calculated for 3Gb/s 64QAM; [3]Assuming RF front-end at carrier frequency of (*N*-1)/2*TTD Range; [4]1-element; [5]BB RX only; [6]Receiving angle; [7]IIP3=OIP3-Conversion Gain; [8]Calculated for receiving angle when signal-to-blocker incidence difference is 90°; [9]RF included, NO ADC.

the processor for the two different pairs of AoA is plotted in Fig. 20(b), where two independent nulls are generated in both the pairs. In both cases, two deep nulls are generated in both the interferences AoA.

The chip is also tested with wideband input signals, in all the processing modes. The wideband input measurement results are shown in Fig. 21(a). In the beamforming mode, frequency-independent roughly 12-dB beamforming gain is observed for a 450-MHz wideband input with AoA $= 60°$. The wide bandwidth in Fig. 21(a) results in TDC performance limitation that folds the distortion components in the desired signal. This problem can be avoided by increasing the TDC operating bandwidth or improving the oversampling ratio in the TDC to avoid noise/distortion folding. In the second mode, two 160-MHz input signals from two different directions are applied to the processor. In this mode, the in-band interference with AoA $= 60°$ is filtered by 24 dB, while the desired signal with AoA $= 10°$ is preserved Fig. 21(b). Finally, in the third mode, the 96-MHz desired signal with AoA $= 0°$ is preserved, while two independent 80-MHz wideband in-band interferences are filtered by more than 21 dB, as shown in Fig. 21(c). In this measurement, one interference is arriving from $-35°$ and the other from $60°$.

The performance of the time-domain SSP is also measured for wide modulated-bandwidth signals, in all the three processing modes. In all three modes, the desired 16-QAM 250-Mb/s signal is applied with one or two interferences. In the beamforming mode, a 12-dB stronger single-tone interference is added to the desired signal and placed in a null AoA of the beamforming pattern. The constellation of the desired signal, before and after enabling the spatial signal processing, at the output of the chip is shown in Fig. 22(a). After beamforming, 5% EVM is calculated for the desired signal. In Fig. 22(b), the constellation of the same desired signal is plotted in presence of a 12 dB stronger 160-MHz wideband interference, before and after enabling the beam-nulling. In this mode, 5.3% EVM is calculated. In the third processing mode, two 80-MHz wideband interferences, each 6 dB stronger than the desired signal power, are added to the desired signal. In this mode, 9.0% EVM is calculated, and the constellation of the

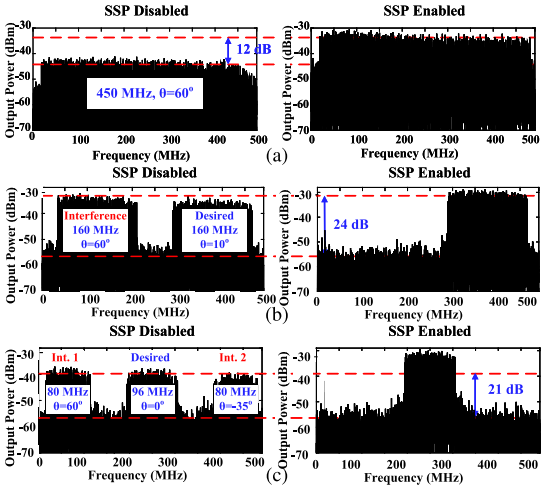


Fig. 21. Measured performance with wideband signals in (a) beamforming mode, (b) beam-nulling mode, and (c) two independent interference cancellation mode.

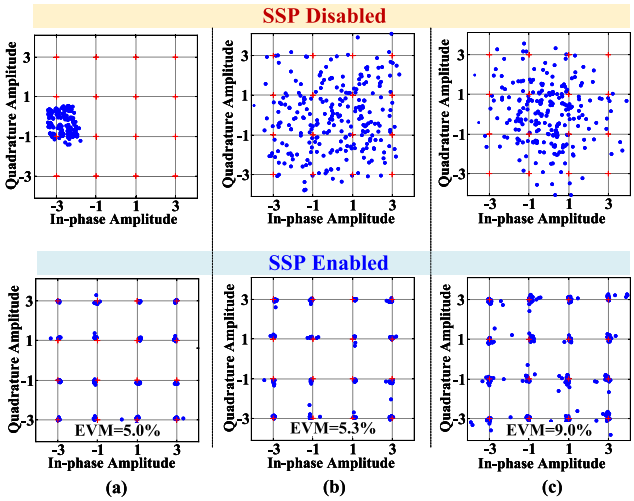


Fig. 22. Measured constellation and EVM of the modulated signal in (a) beamforming mode, (b) beam-nulling mode, and (c) two independent interference cancellation mode.

desired signal is shown in Fig. 22(c). The modulated signals' performance in all the processing modes proves the applicability of the proposed SSP for high-speed wireless links.

The four-element BB discrete-time SSP consumes 40-mW power (25 mW for the signal combination through the time-interleaved VTCs, 12 mW for TDC quantization, and 3 mW for sample phase generation using controlled delay lines). The input 1-dB compression point (P1 dB) of this SSP is -0.5 dBm from the desired signal perspective, and its IIP3 is 7.9 dBm. In Table I, the BB time-domain SSP is compared with the state-of-the-art. The implemented delay range of 1 ns allows the RF-FE to work at center frequencies as low as 1.5 GHz, resulting in $>33\%$ fractional bandwidth for this design.

V. Conclusion

This work presents a BB discrete-time time-domain SSP that presents a time-based system-level design approach for wideband beamforming, beam-nulling, and independent filtering of multiple interferences. The time-domain design offers TTD-based processing, which results in high fractional bandwidth capability. This design is also the only solution with multiple interference cancellation and embedded ADC. Time amplification linearity enhancement was presented by combining different time amplifier structures. The time-domain processor chip was fabricated, and its functionality was proven through various measurements. Wideband frequency-independent BB spatial processing, in the beamforming, beam-nulling, and two independent interference cancellation modes was validated by applying swept single-tone, wideband, and modulated signals to the chip. In the end, the measurement results of the fabricated chip were compared with the state of the art.

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