An Integrated Discrete-Time Delay-Compensating Technique for Large-Array Beamformers

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***Abstract*— This paper implements a wide aperture high-resolution true time delay for frequency-uniform beamforming gain in large-scale phased arrays. We propose a baseband discrete-time delay-compensating technique to augment the conventional phase-shift-based analog or hybrid beamformers. A generalized design methodology is first developed to compare delay-compensating analog or hybrid beamforming architecture with their digital counterpart for a given number of antenna elements, modulation bandwidth, ADC dynamic range, and delay resolution. This paper shows that delay-compensating analog or hybrid beamformers are more energy-efficient for high dynamic-range applications compared to true-time-delay digital beamformers. To demonstrate the feasibility of our proposed technique, a four-element analog delay-compensating baseband beamformer in 65-nm CMOS is prototyped. A time-interleaved switched-capacitor array implements the discrete-time delay-compensating beamformer with a wide delay range of 15-ns and 5-ps resolution. Measured power consumption is 47 mW with frequency-uniform array gain over 100-MHz modulated bandwidth, independent of angle of arrival. The proposed delay compensation scheme is scalable to accommodate the delay differences for large antenna arrays with higher range/resolution ENOB compared with prior art.**

***Index Terms*— Multiple-input and multiple-output (MIMO), beam squinting, 5G, time-interleaving, true-time delay, modulated bandwidth, large scale arrays, discrete-time analog processor.**

I. Introduction

THE dramatic growth in information data rates in the past decade are driving research and development of high data-rate energy- and spectral-efficient communication networks [1]–[3]. This unmet need to support larger capacities has led to deployment of dense networks using small-cell technology, large antenna arrays employing beamforming, and wide modulated bandwidths (BW) at sub-6GHz and millimeter-wave (mm-wave) frequencies in applications such as fifth-generation wireless (5G) [4], and satellite communications [5].

This work focuses on hardware architectures for beamforming. These architectures can be broadly classified as analog [6]–[8] or digital [9], depending on the application of beamforming in the signal path. In the analog domain, the necessary phase-shift is implemented at the mm-wave or RF, LO or baseband (BB). Irrespective of the implementation, the current state-of-the-art in array signal processing are dominated by phase-shifters (PS). PS-based beamformers have been well known for over a century, largely employed for radar systems to overcome path loss and enable advanced signal processing [10]. They are popular, and adequate so far, because the modulation BWs have been relatively smaller, and the number of antenna elements is limited in the array. In such a narrow-band system, a time delay can be approximated by an angular phase shift [7]. However, for a system with either wide modulated BWs or a large number of antennas, this approximation is not valid and causes beam squinting [11]–[14]. Therefore, for next-generation wideband wireless networks, a true-time-delay (TTD) is necessary to accommodate the delay differences for larger antenna arrays and achieve uniform beamforming gain over wide modulated BW [11]. In a prior-work [14], we demonstrated a TTD at BB using a discrete-time delay-compensating technique for spatial interference cancellation. In this work, we propose a discrete-time delay-compensating technique to implement the TTD at BB for beamforming. Following are the contributions of the proposed work compared to prior-art and [15]:

1) Beam squinting and frequency-dependence of beamforming gain is described in prior PS-based beamformers, thereby explaining the need for TTD based beamformer (Section II).
2) A generalized design methodology for discrete-time N-element analog/hybrid beamformers is presented, and the discrete-time delay compensating technique of [15] is leveraged for beamforming (Section III).

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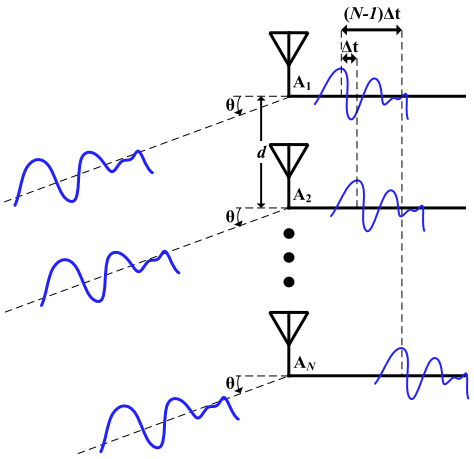

Fig. 1. Model of an N-element array.

3) Design considerations and comparisons are presented for analog/hybrid and digital delay-compensating techniques in area and power consumption, (Section III) and
4) A proof-of-concept prototype for a 4-element analog beamformer with discrete-time delay-compensating elements is implemented in 65 nm CMOS and the measured results demonstrate a sampled time-delay based frequency-uniform beamforming across 100 MHz modulated BW with 15 ns range and 5 ps resolution (Section IV). To the best of our knowledge, this is the largest range/resolution ratio exceeding prior art by more than 4.4 bits. This proposed BB implementation permits compatibility to various RF front-ends.

II. PS-Based vs TTD-Based Beamformers

Beamforming, beam squinting, and phased-arrays have been described in detail in [7]–[9], [11], [12], [14]–[18]. Herein, we briefly revisit the basic concepts to establish that the popular PS-based beamformers are inadequate, and TTD-based beamformers are needed, to avoid beam squinting for a large number of antennas (e.g., in massive MIMO base stations), wide modulated bandwidths (in next-generation communication standards), and large angle of arrival (AoA) coverage.

Consider an N-element linear phased array receiver (RX) model in Fig. 1, with an inter-element time-delay modeled as:

$$\Delta t = \frac{d}{\lambda_C} \cdot \frac{\sin(\theta)}{f_C} \tag{1}$$

where, Δt and d are the time delay and the distance between two consecutive antennas, respectively, θ is the AoA, and λ_C is the wavelength corresponding to the center frequency, f_C. A beamforming RX first compensates this time delay and then adds the aligned signals for beamforming. In a narrowband system, this time delay is approximated by an angular phase shift [7] (Fig. 2(a)). The normalized beamforming gain (Gain/N) in a PS-based RX can be written as (2). Since the phase shift unit, ($\Delta\varphi$), is independent of frequency, f, the normalized gain is frequency-dependent.

$$(\text{Gain}/N)_{\text{PS}} = \frac{1}{N}\sum_{l=0}^{N-1}\left|e^{j(2\pi f \cdot l \cdot \Delta t - l \cdot \Delta\varphi)}\right| \tag{2}$$

The normalized beamformer gain (Gain/N) is plotted versus normalized frequency (f/f_C) for $\theta = 45°$ in Fig. 2(a). It is observed that the normalized 3dB bandwidth ($\text{NBW}_{3\text{dB}}$ – normalized frequency range where the normalized beamformer gain drops by 3 dB) becomes smaller with an increasing number of antennas in a PS- based beamformer as illustrated in II(a). While not an issue for small N, the frequency-dependent gain becomes more severe in large-array transceivers supporting large array applications with wide modulated BWs (Fig. 3), as described in [14].

As proven in [16], [17], for large values of N, the $\text{NBW}_{3\text{dB}}$ is given as:

$$\text{NBW3dB} = \frac{0.886}{N \cdot \left(\frac{d}{\lambda_C}\right)|\sin(\theta)|} \tag{3}$$

Thus, for a system with wide modulated BWs, a large number of antennas, or AoA near its worst cases (i.e. $\theta = -60°$ or $60°$), beam squinting is experienced in a PS-based beamformer (Fig. 2(a)). This frequency-dependent beamforming gain acts as a bandpass filter and introduces distortion and degrades desired signal-to-noise ratio (SNR).

In contrast, a TTD-based beamformer (Fig. 2(b)) avoids this problem as the gain is fundamentally independent of frequency and AoA even for a large N.

Because the delay-compensation at RF is equivalent to its implementation in the BB after the downconversion mixer and a phase shift, the TTD-based beamformer can be realized through delay-compensation in RF or BB as shown in Fig. 4(a). Various implementations for the required TTD and phase shift are also shown in Fig. 4(b). Delay-compensation in RF is difficult to implement without severe penalty in linearity, noise, area, and tunability. TTD elements implemented using inductive delay lines at RF in [13], [19] consume area, and are susceptible to variation over process corners. Moreover, an active all-pass filter based delay implementation requires high power consumption and suffers from a mismatch in RF [20]. In [12] a 16-element digital TTD beamforming RX has been integrated. Beam squinting is solved in the digital domain using digital TTD and fractional-rate sampling. However, 16 ADCs increase the overall power consumption of the RX significantly.

We propose to implement the TTD in analog BB using a discrete-time technique [15] described in the next section to mitigate beam squinting. This array is designed to augment the conventional PS-based analog or hybrid beamformers especially for larger arrays with higher modulated bandwidths (where beam squinting is more severe). Since the beamforming is done at BB, the RF-FE must have sufficient linearity to downconvert the signal. We assume that further RF-FE impairments, especially amplitude and phase mismatches between the channels, can be taken into design considerations so as to not limit the performance of the beamformer. These mismatches can be reduced using digital techniques similar to improving the image rejection ratio in a quadrature RX for intra-band carrier aggregation [21], [22]. The idea of delay compensation proposed herein can be used in MIMO receivers, with multiple outputs (not just one in the beamformer case).

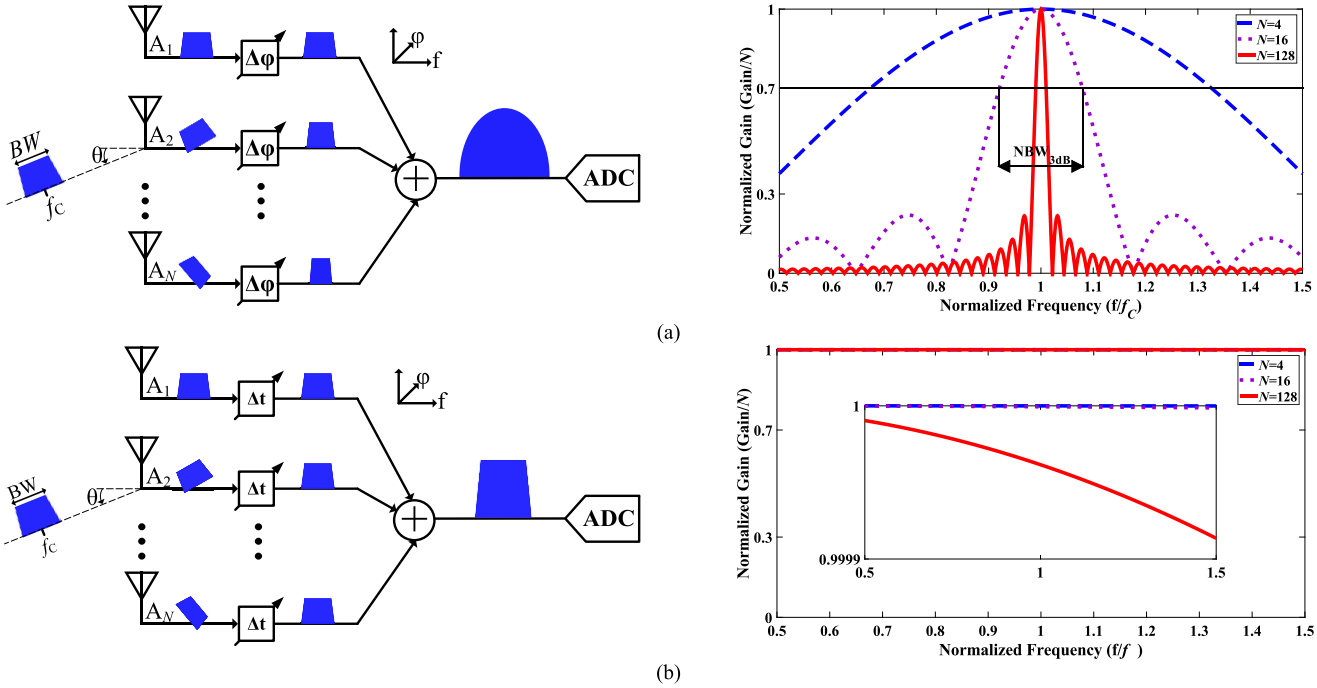

Fig. 2. Simplified beamformer and its frequency response in: (a) phase-shifter (PS)-based system, and (b) true-time-delay (TTD)-based system.

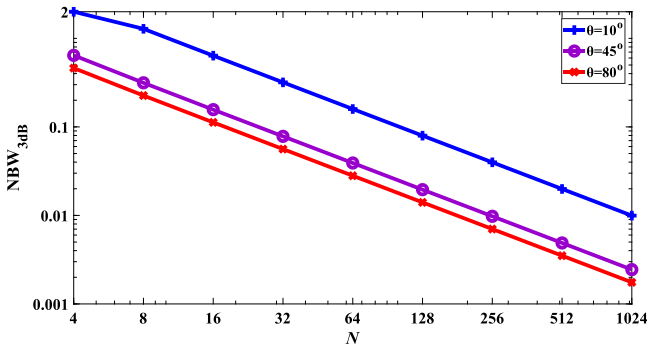

Fig. 3. Simulated normalized 3dB bandwidth (NBW_{3dB}) of a PS-based N-element antenna array plotted against N.

In that multi-output scenario, frequency-independent beam-nulling [15] or multi-beam receiver can be implemented. Given the large optimization space for hardware design in MIMO applications with large arrays (such as massive MIMO), a design methodology encompassing the trade-offs with large antenna arrays or wide modulated BWs is next presented.

III. Design Considerations for the Proposed TTD-Based Beamformers

A. The Proposed Discrete-Time Delay-Compensating Element for an N-Element Beamformer

Fig. 5 shows the proposed discrete-time delay compensation technique where the down-converted and phase- shifted signals from N antennas are sampled at different time instants using a switched-capacitor array (SCA) [15]. The sampled values stored on the capacitors are then added using a switched-capacitor based summer as shown in Fig. 6. The transconductance amplifier (OTA) used in this summer must satisfy the SNR and modulated BW requirements of the down-converted signal. The switched-capacitor based implementation of a beamformer requires N phases for sampling ($\varphi_{1...N}$) followed by addition (σ) and reset (RST) phase, in an N-element array. In the sampling phase, $\varphi_{1...N}$, an input signal from each RX is first sampled on a sampling capacitor (C_S) uniquely. The value of C_S is determined by the thermal noise requirements. After the last sampling phase (φ_N), the stored charges on each capacitor are shared in the σ phase. This charge sharing performs an averaging function. To change this functionality to summation and form the beam, the shared charges are transferred to the feedback capacitor (C_F) in a switched-capacitor summer following the SCA. After forming the beam, the summer is reset by the RST phase to prepare for the next sample. For proper functionality, σ should be non-overlapping with all the sampling phases ($\varphi_{1...N}$) and the RST phase. To compensate the time delay between the N inputs (from N-elements) in this SCA, each signal must be sampled at a distinct time instant. This technique ensures that the time delay between two consecutive sampling phases (φ_i and φ_{i+1}) is the same as the time delay between the corresponding inputs.

The non-overlapping condition on the sampling and RST phases with σ presents unique implementation challenges in this delay-compensating architecture. To overcome this challenge, both the sampling ($\varphi_{1...N}$) and addition phases (σ) are further time-interleaved to M phases. The period of each time-interleaved phase is set to M times of the initial phase period. Note that adding sampled input signals, which are sampled by these interleaved phases, is equivalent to sampling them

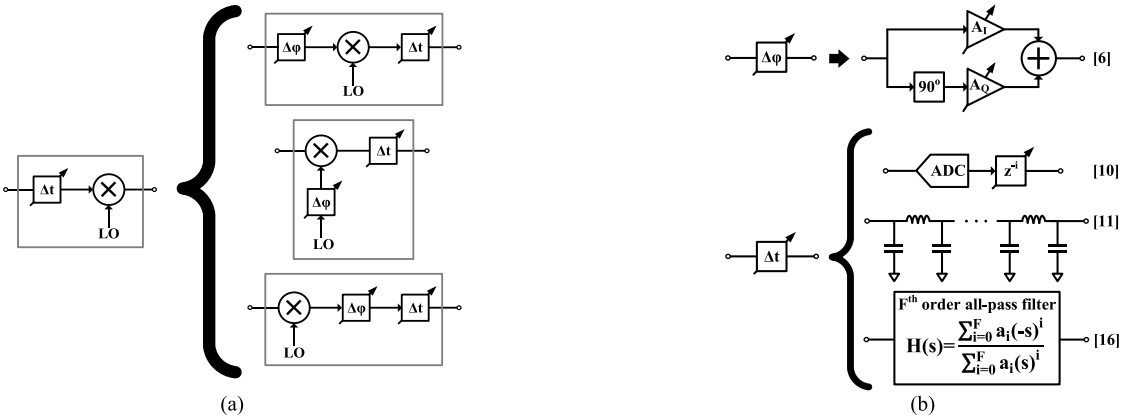

Fig. 4. Equivalent implementations of: (a) RF TTD, and (b) Phase shifter and time delay unit.

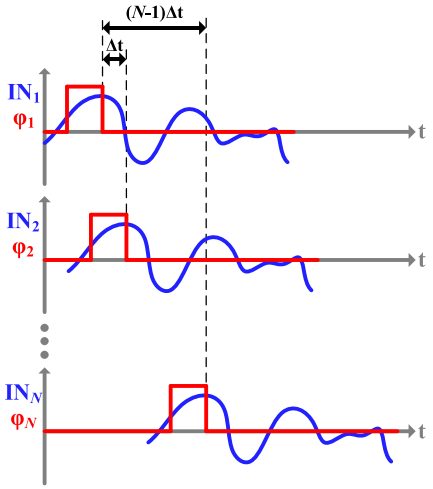

Fig. 5. Sampling-based discrete-time delay compensation.

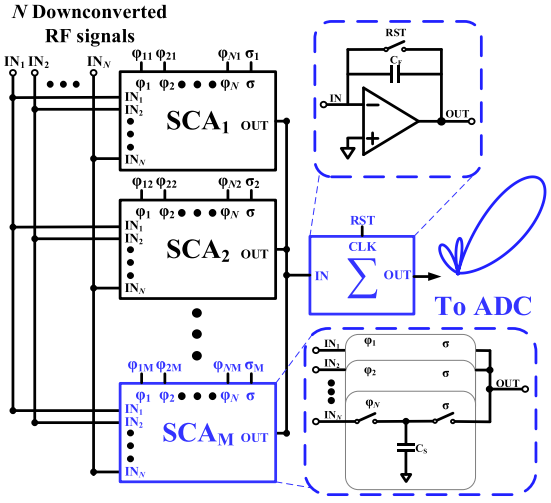

Fig. 6. System diagram of the proposed analog delay-compensation element with switched-capacitor array (SCA) and adder (in the inset). RF front-end and the ADC are not implemented.

with the initial non-interleaved clock phase. Fig. 6 shows the overall implementation of a discrete-time delay compensation beamformer for an N-element antenna array.

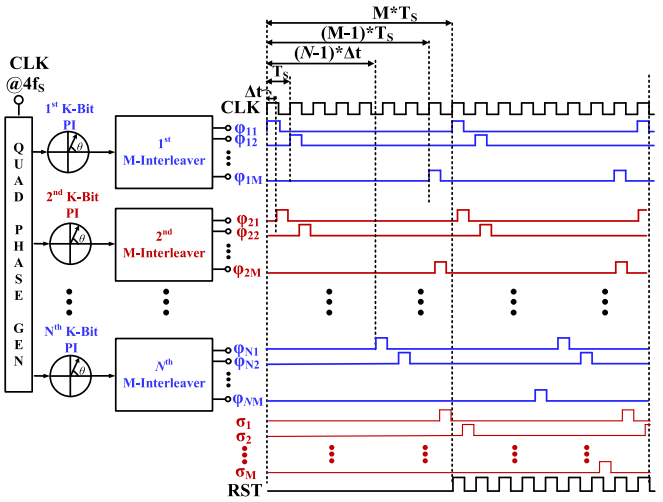

Fig. 7. The proposed clock generation unit with the timing diagram for the SCA in Fig. 6.

The required phases in this architecture with an interleaving factor of M is shown in Fig. 7. To generate these required phases, a clock generation unit for the discrete-time delay-compensating element is also shown in Fig. 7. Each antenna requires a K-Bit phase interpolator (PI) to delay the corresponding sampling phase. The K-bit PI is implemented using 2^K inverter-based units adapted from [23] and described in detail in [15]. The delayed clock after the PI is fed to an M-phase interleaver to generate the M interleaved phases. The M-phase interleaver reduces the input clock frequency by a factor of M and is simply implemented through M units of static AND gates and registers.

As discussed in Section II, larger arrays or wider modulated BWs increase the sampling frequency for interleaving. Consequently, the closed-loop bandwidth of the summer will increase resulting in higher power consumption. The design also needs to consider the total number of sampling capacitors ($=N \cdot M$). A higher M increases the capacitive load on the RF front-end RX. For larger arrays, the requirement on resolution and jitter of the clock generation unit gets more strict, resulting in higher clocking power, besides the increase in the number of PIs and level of interleaving. A generalized

design methodology using the proposed SCA for an N-element analog beamforming RX is next described.

B. Generalized Design Methodology for an N-Element Analog Beamformer With a Single-ADC

The maximum time delay in an N-element antenna array is the delay between the received signals at the first and the last (N^{th}) antenna. This time delay is expressed as:

$$\Delta t_{\max} = (N-1)\cdot \Delta t|_{\theta=\pm 60} = \frac{\sqrt{3}}{2}\cdot (N-1)\cdot \frac{d}{\lambda_C}\cdot \frac{1}{f_C} \quad (4)$$

$\Delta t_{\max}$ must be compensated through the time-interleaved implementation. At the same time, the maximum delay compensation ($T_{C-\max}$) achieved in this architecture can be written as (5):

$$T_{C-\max} = (M-1)\cdot T_S = (M-1)/f_S \quad (5)$$

where T_S and f_S are the reference clock period and sampling frequency, respectively. To cover the entire 120° range, $T_{C-\max}$ should be larger than $\Delta t_{\max}$ resulting in (6):

$$T_{C_{\max}} \geq \Delta t_{\max} \rightarrow T_S \geq \frac{\frac{\sqrt{3}}{2}\cdot (N-1)}{(M-1)}\cdot \frac{d}{\lambda_C}\cdot \frac{1}{f_C} \quad (6)$$

Considering a low-IF RX architecture, the downconverted signal covers the frequency range of DC to modulated BW.

Perfect sampled signal reconstruction within this BW must satisfy the Nyquist condition as follows:

$$f_S \geq 2BW \rightarrow ?T_S \leq \frac{1}{2BW} \quad (7)$$

Substituting (6) in (7) yields the following:

$$\frac{\frac{\sqrt{3}}{2}\cdot (N-1)}{(M-1)}\cdot \frac{d}{\lambda_C}\cdot \frac{1}{f_C} \leq \frac{1}{2BW}$$

$$M \geq 1 + \left(\frac{d}{\lambda_C/2}\right)\cdot \frac{\sqrt{3}}{2}\cdot (N-1)\cdot \left(\frac{BW}{f_C}\right) \quad (8)$$

For any N-element antenna array with antenna spacing d, and fractional modulated bandwidths of BW/f_c, the relationship between the required sampling frequency (f_S) and the interleaving factor (M) in an analog delay-compensation architecture (Fig. 6) is found to be:

$$f_S = 2\ BW \quad (9)$$

$$M = 1 + \left\lceil \left(\frac{d}{\lambda_C/2}\right)\cdot \frac{\sqrt{3}}{2}\cdot (N-1)\cdot \left(\frac{BW}{f_C}\right)\right\rceil \quad (10)$$

where $\lceil \ldots \rceil$ is the ceiling function to find the smallest integer M that satisfies (8).

The required interleaving factor for three different number of antennas ($N = 4$, 16, 128) is plotted against fractional BW in Fig. 8. For a smaller number of antennas or lower fractional BW, the interleaving factor can be set equal to the minimum value ($M = 2$). As the number of antenna or fractional BW increases, the required interleaving factor also increases as given by (10).

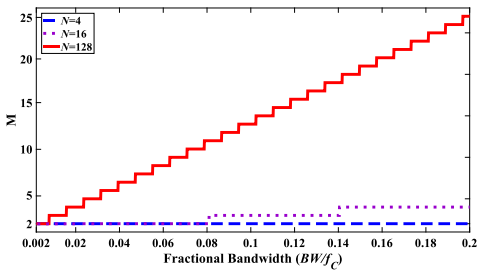

Fig. 8. Relation of interleaving factor (M) with fractional bandwidth for a different number of antennas (N) in an analog discrete-time delay compensation beamformer.

We next estimate the power consumption and occupied area to realize a delay-compensation based analog beamformer (Fig. 9(a)) with an ADC resolution of R-Bit. The DC gain (A_0) and the unity-gain bandwidth (ω_u) requirements of the OTA used in the SCA are found to be:

$$A_0 \geq N\cdot 2^{R+1} \quad (11)$$

$$\omega_u \geq 2^*\ln(2)^*\ N\cdot (R+1)\, f_S \quad (12)$$

It is observed in (11) and (12) that both the ω_u and A_0 are directly proportional to the number of antenna elements. Neglecting parasitics, second order effects, and considering a two-stage internally-compensated OTA, the transconductance of this OTA can be designed to be linearly dependent to the DC current. As a result, the DC gain of the OTA is independent of the DC current and its power consumption (P_{OTA}). At the same time, ω_u is a linear function of the OTA transconductance, and thus varies proportionally to P_{OTA}. Furthermore, as the transistors' width is designed to proportionally depend on the DC current (to make OTA's transconductance linearly dependent to the DC current), the OTA area (S_{OTA}) can also be approximated as a linear function of P_{OTA}. Given these assumptions, the minimum requirement on the OTA ω_u from (12) results in linear dependency of P_{OTA} and S_{OTA} to the product of the number of antennas and sampling frequency, as shown in (13):

$$P_{OTA} \approx P_{OTA0}\cdot N\cdot f_S$$

$$S_{OTA} \approx S_{OTA0}\cdot N\cdot f_S \quad (13)$$

where P_{OTA0} and S_{OTA0} are power consumption and area of an OTA designed for a single-element array with a unit sampling frequency (1 Hz).

The area of the SCA, S_{SCA} is dictated by the sampling capacitors, C_s and can be approximated as a linear function of N and C_S as shown below:

$$S_{SCA} \approx S_{C0}\cdot N\cdot C_S \quad (14)$$

where S_{C0} is the area of unit capacitance in the technology.

The total area of all the SCAs ($S_{\sum SCA}$) can be derived as:

$$S_{\Sigma SCA} \approx S_{C0}\cdot (N\cdot M\cdot C_S + C_F) \xrightarrow{C_S=C_F=C}$$

$$S_{\Sigma SCA} \approx S_{C0}\cdot (N\cdot M+1)\cdot C \quad (15)$$

In our implementation, the PI is a dominant contributor to the overall area and power consumption and hence, merits

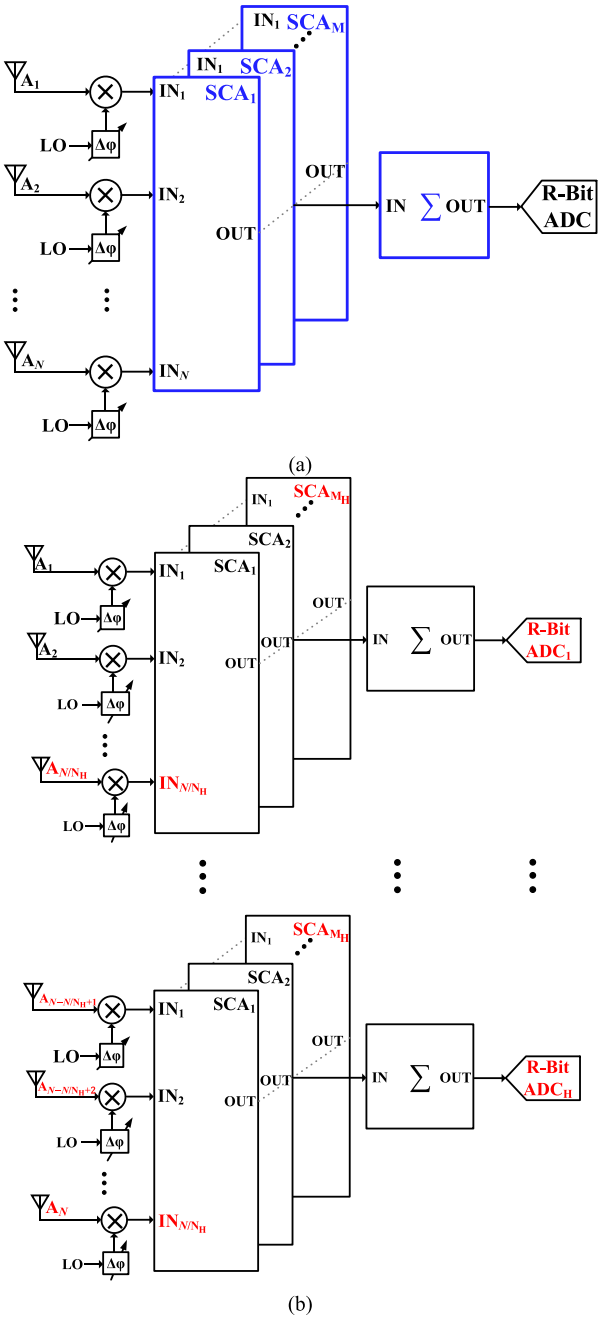

Fig. 9. Analog discrete-time delay compensation implementation for: (a) Analog beamformer; (b) Hybrid beamformer.

careful attention in the system-level design considerations. The clock power (P_{CLK}) and area (S_{CLK}) can be approximated as:

$$\begin{aligned} P_{CLK} &\approx P_{K\text{-}PI0} \cdot N \cdot f_S \\ S_{CLK} &\approx S_{K\text{-}PI0} \cdot N \end{aligned} \tag{16}$$

where $P_{K\text{-}PI0}$ and $S_{K\text{-}PI0}$ are power consumption at the unit frequency of 1 Hz and area of a K-Bit PI clocking, respectively.

As seen in (11), (12), and (13), the requirement for OTA's A_0 and ω_u (both proportional to N) can demand stringent design requirements for larger arrays which may not even be feasible. Thus, analog beamforming, while efficient with a single-ADC, may not be suitable in larger arrays for mm-wave massive MIMO. As an alternative, hybrid delay-compensating beamforming (Fig. 9(b)) is a promising candidate in these cases to relax the requirements [6]. In a hybrid implementation, the array is divided into N_H sub-arrays. Analog beamforming is performed on each sub-array and sub-arrays' beams are fed to digital beamforming, where the TTD is implemented in the digital domain. By substituting N/N_H with N in (10), where N_H is the number of ADCs, the new interleaving factor (M_H) can be rewritten as (17):

$$M_H = 1 + \left\lceil \left(\frac{d}{\lambda_C/2}\right) \cdot \frac{\sqrt{3}}{2} \cdot \left(\frac{N}{N_H} - 1\right) \cdot \left(\frac{BW}{f_C}\right) \right\rceil \tag{17}$$

In hybrid beamforming, as the number of ADCs is increased to N_H, the OTA requirements, in (11) and (12), will equivalently relax by an N_H factor and will be the same in requirements as in the case of number of antennas being N/N_H (assuming N/N_H is an integer). This relaxes the overall power consumption and area of the OTAs to be approximately the same as that of an analog beamformer, expressed in (13).

The above analysis is further expanded to compute the area requirements of the hybrid delay-compensating beamformer. Corresponding to each ADC/OTA, there are M_H SCAs with N/N_H inputs. Using (14), the capacitive area in hybrid delay-compensating beamformer ($S_{\sum SCAH}$) can be written as (18). For small values of N_H, the area occupied by the SCA capacitors in the hybrid delay-compensating beamformer can be approximated to be the same as analog delay-compensating beamformer over N_H.

$$\begin{aligned} S_{\Sigma SCAH} &\approx N_H \cdot S_{C0} \cdot \left(\frac{N}{N_H} \cdot M_H + 1\right) \cdot C \\ &\approx S_{C0} \cdot N \cdot M_H \cdot C \\ \xrightarrow{M_H \approx M/N_H} S_{\Sigma SCAH} &\approx S_{C0} \cdot \frac{N \cdot M \cdot C}{N_H} \end{aligned} \tag{18}$$

The hybrid delay-compensating beamforming architecture reduces the number of the PIs to N/N_H and also relaxes P_{CLK} and S_{CLK} compared to that of an analog beamformer by a factor of N_H. However, the number of ADCs correspondingly increases by N_H leading to an increase in the overall area/power of the ADCs by N_H.

Digital delay-compensating beamformer can be seen as a hybrid delay-compensating beamformer with N ADCs ($N_H = N$). In this case, there will be N OTAs (used in the sample and hold circuit prior to the ADC) with the total area (S_{OTA}) and power consumption (P_{OTA}) similar to that in an analog delay-compensating beamformer. Because there is no analog delay-compensation, no PIs are required in digital beamforming, saving the area/power consumption from the PIs. However, the equivalent increase in the ADCs by a factor of N adds significant power/area penalty. Note that in this paper we assume that the data conversion dynamic range is limited to in-band interference power and consequently the ADC resolution is constant, independent from beamformer implementation. TABLE I compares the analog/hybrid/digital beamforming implementations, in terms of estimated power consumption and area (ignoring second order effects) and provides guidelines to choose the most suitable

TABLE I
DELAY-COMPENSATING ANALOG AND HYBRID BEAMFORMERS COMPARED TO DIGITAL BEAMFORMERS

	Analog	Hybrid	Digital
P_{OTA}	$P_{OTA0}\cdot N\cdot f_S$	$P_{OTA0}\cdot\left({}^{N}/_{N_H}\right)\cdot f_S$	$P_{OTA0}\cdot f_S$
S_{OTA}	$S_{OTA0}\cdot N\cdot f_S$	$S_{OTA0}\cdot\left({}^{N}/_{N_H}\right)\cdot f_S$	$S_{OTA0}\cdot f_S$
# OTA	1	N_H	N
# PI	N	${}^{N}/_{N_H}$	0
# ADC	1	N_H	N
Overall Power	$P_{OTA0}\cdot N\cdot f_S + P_{K\text{-}PI0}\cdot N\cdot f_S + P_{R\text{-}ADC}$	$P_{OTA0}\cdot N\cdot f_S + \left({}^{N}/_{N_H}\right)\cdot P_{K\text{-}PI0}\cdot f_S + N_H\cdot P_{R\text{-}ADC}$	$P_{OTA0}\cdot N\cdot f_S + N\cdot P_{R\text{-}ADC}$
Overall Area	$S_{OTA0}\cdot N\cdot f_S + S_{C0}\cdot(N\cdot M+1)\cdot C + N\cdot S_{K\text{-}PI0} + S_{R\text{-}ADC}$	$S_{OTA0}\cdot N\cdot f_S + S_{C0}\cdot\frac{N\cdot M\cdot C}{N_H} + \left({}^{N}/_{N_H}\right)\cdot S_{K\text{-}PI0} + N_H\cdot S_{R\text{-}ADC}$	$S_{OTA0}\cdot N\cdot f_S + N\cdot S_{R\text{-}ADC}$

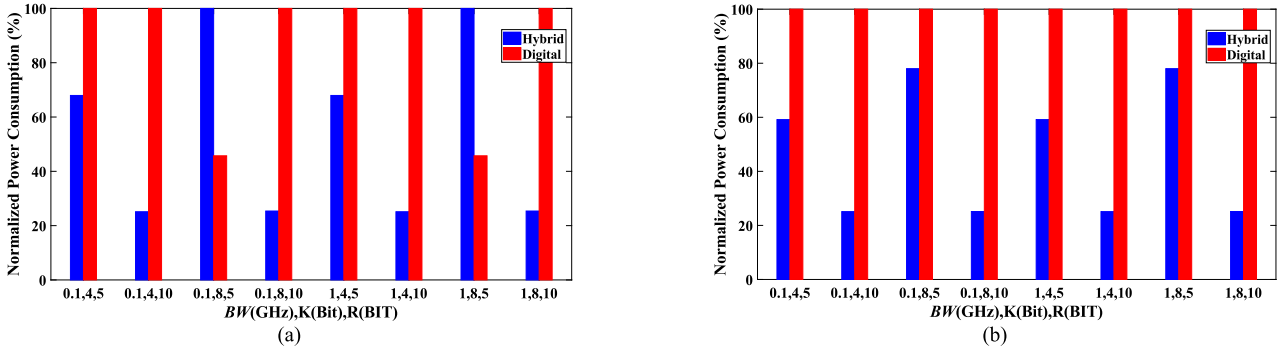

Fig. 10. Comparison of normalized power consumption against different combinations of bandwidth (BW), PI resolution (K), and ADC resolution (R) for (a) N = 16, and (b) N = 128, assuming power consumed in a 65 nm CMOS process for 8-bit PI as 44 mW/200 MHz, 5-bit OTA as 3 mW/4 Inputs/100 MHz, and 5-bit ADC (described in [26]) as 1.2 mW/250 MHz.

beamformer implementation. In TABLE I, the digital post-processing power and area is not accounted, thereby favoring the digital beamformer in the comparison, since the entire TTD has to be implemented in the digital domain. Normalized power consumption in analog/hybrid implementation and digital implementation, for 16 scenarios, are compared in Fig. 10. The baseline power consumption for different circuits assumed in Fig. 10 shows that for higher ADC resolution (R), the power consumption of the digital beamforming is much higher than corresponding analog/hybrid implementation. However, for lower ADC resolutions, the dominating factor is the PI resolution (K). The ADC power is assumed to increase linearly with sampling frequency and 4× for every additional bit increase in the resolution [24]. If the exponent of scaling of ADC power consumption with the sampling frequency is larger than unity [24], it will further benefit the analog/hybrid architecture in our comparative discussion.

IV. DESIGN AND MEASUREMENTS OF A 4-ELEMENT DELAY-COMPENSATING BEAMFORMER

A 4-element analog delay-compensating beamforming architecture with 100 MHz BW is fabricated in a 65 nm CMOS as a proof of concept. A BW of 100 MHz is chosen due to limitations in OTA gain-bandwidth, PI frequency, and measurement setup. The implemented design achieves a maximum 15 ns delay between the first and the last antenna. The proposed time-interleaved clocking scheme compensates this delay with a resolution of 5 ps and covers the entire ±60° angle-of-arrival through the proposed true-time-delay compensation. Thus ±60° AoA range corresponds to ±15 ns delay between the first and the last antenna.

The minimum sampling frequency for perfect signal construction is set to 200 MHz in the SCA and the PIs. The PI resolution is selected as 8-bit to demonstrate the scalability of the PI for applications requiring higher precisions. The clock generator in Fig. 7 obtains resolution of 5 ps and a range of 15 ns in the sampling clock phases and feeds 16 clock phases to the SCA shown in Fig. 6 (M = 4). The quadrature phase generator in the clock generator provides quadrature outputs at 200 MHz with complete cycle coverage (=360°) and period of T_S = 5 ns. Each quadrature phase is capable of 5 ps resolution (=1.25 ns/256) which is determined by the 8-bit phase interpolator (PI). The 5 ns range is realized using a 2-bit 4:1 quadrant select multiplexer that acts on the four differential quadrature outputs of the PI.

Because the period of the 200 MHz clock is insufficient to cover the required time span of 15 ns between the first and the last antenna, we generate four phases (φ_{11}, …, φ_{14}), for each quadrant select MUX, at 50 MHz with a 12.5% ON-time from a time interleaver leading to a total of 16 phases (φ_{11}, …, φ_{44}) as shown in Fig. 7. Though M = 2 is sufficient to cover entire fractional BW less than 20% as illustrated in Fig. 8, a 4× interleaving factor is employed for showing the scalability of the proposed delay-compensating architecture for *BW* up to 100 %.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR-ART TTD BASED BEAMFORMERS IMPLEMENTATIONS

	JSSC2017 [20]	**IMS2015** [19]	**RFIC2018** [13]	**JSSC2015** [27]	**RFIC2018** [12]	**Proposed Work**
Approach	Gm-C[a]	Delay line[a]	LC delay[a]	Gm-C	Delta-Sigma	**BB Discrete-Time Delay-Compensation**
# Channel	-	-	-	4	16	**4**
# Beam	-	-	-	1	4	**1**
Tech. (nm)	CMOS (130)	CMOS (130)	BiCMOS (130)	CMOS (140)	CMOS (40)	**CMOS (65)**
VDD (V)	1.4	1.2	2.5	1.5	N/R[c]	**1.0**
Delay Range (ps)	1450	400	508	550	7500	**15000**
Delay Resolution (ps)	10	5	4	13	500	**5**
ENOB Log_2 (Range/Res)	7.2	6.3	7.0	5.4	4	**11.6**
Frequency Range (MHz)	1900 (RF)	19000 (RF)	18000 (RF)	1500 (RF)	100 (DIG-BB)[e]	**100 (ANA-BB)[f]**
Area (mm^2)	0.6	4	5.45	1	0.29	**0.57 (active)**
Power	112-364mW[b]	2.6-6mW[a]	285mW[a]	450mW[b]	453mW	**Analog: 3mW/100MHz Clock: 44mW Total: 47mW**

[a] Delay-line implementation only, [b] Including RF-FE, [c] Not reported, [d] Not applicable, [e] DIG-BB: Digital baseband, [f] ANA-BB: Analog baseband.

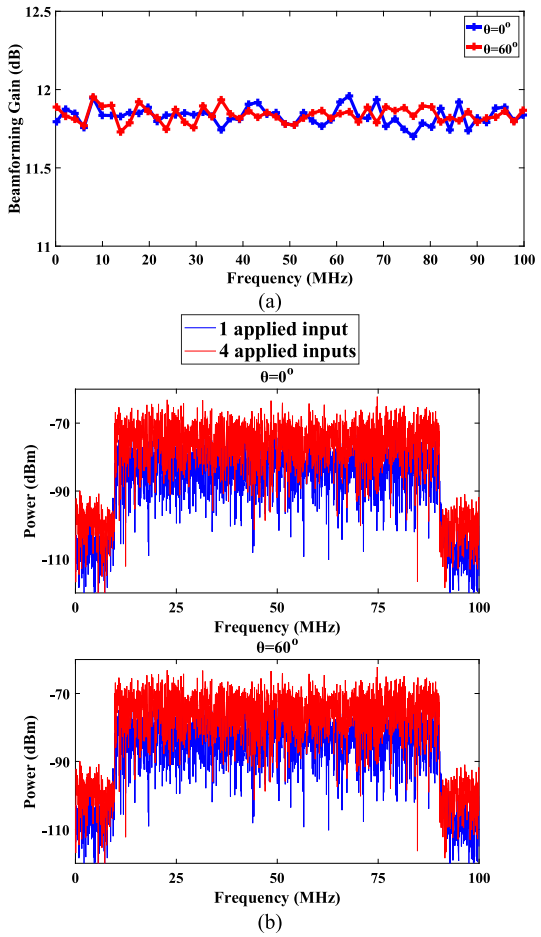

Fig. 11. Simulation results for: (a) beamforming gain for a single-tone signal for two different AoAs, and (b) 80 MHz BW signal for two different AoAs.

As shown in Fig. 11, the simulated beamforming gain (defined as the ratio of the output power when all the 4 inputs are applied to the output power when only one input is applied) is uniform for different AoA across the entire band.

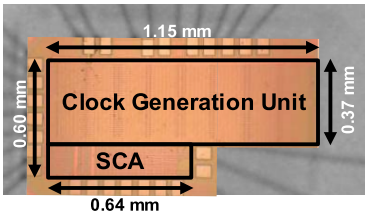

Fig. 12. Die micrograph in 65nm CMOS with chip-on-board bond wires (die micrograph is overlaid on the encapsulated chip).

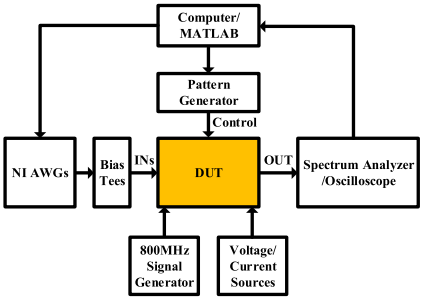

Fig. 13. Test setup for the fabricated 4-element prototype.

The fabricated prototype chip occupies a core area of 0.57 mm^2 in 65 nm TSMC technology (Fig. 12). The test setup including the prototype device is shown in Fig. 13. The input signals to the chip are generated through two NI PXIe-5450 arbitrary (145 MHz modulated BW) waveform generators with four independent differential channels.

The applied delay to the SCA is programmed to be proportional to antenna spacing of $\lambda_{min}/2$ where λ_{min} is the wavelength corresponding to the highest frequency in the band (100 MHz). Quadrature phases at 200 MHz are generated on-chip from an off-chip 800 MHz signal generator. The digital power consumption including the clock generation unit with four PIs and interleaving units (M = 4, N = 4) is 44 mW at 1.0 V supply. This power can be easily scaled down with supply, CMOS process or required resolution

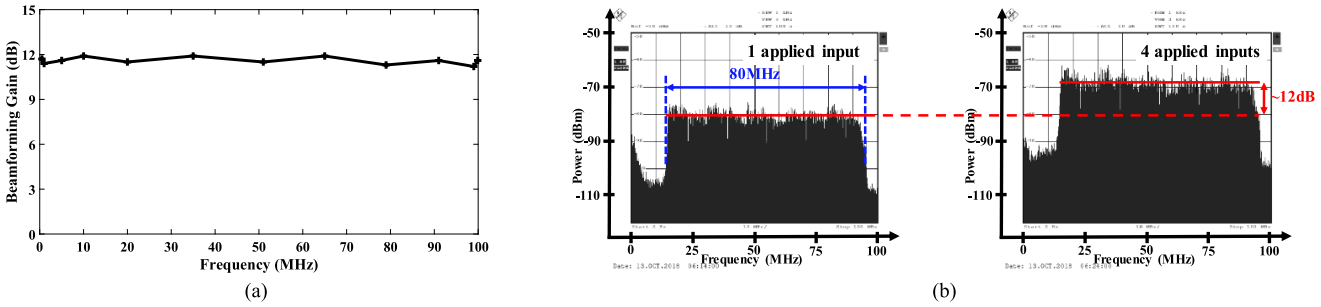

Fig. 14. Measurement results for: (a) beamforming gain for a single-tone signal, and (b) 80 MHz BW signal.

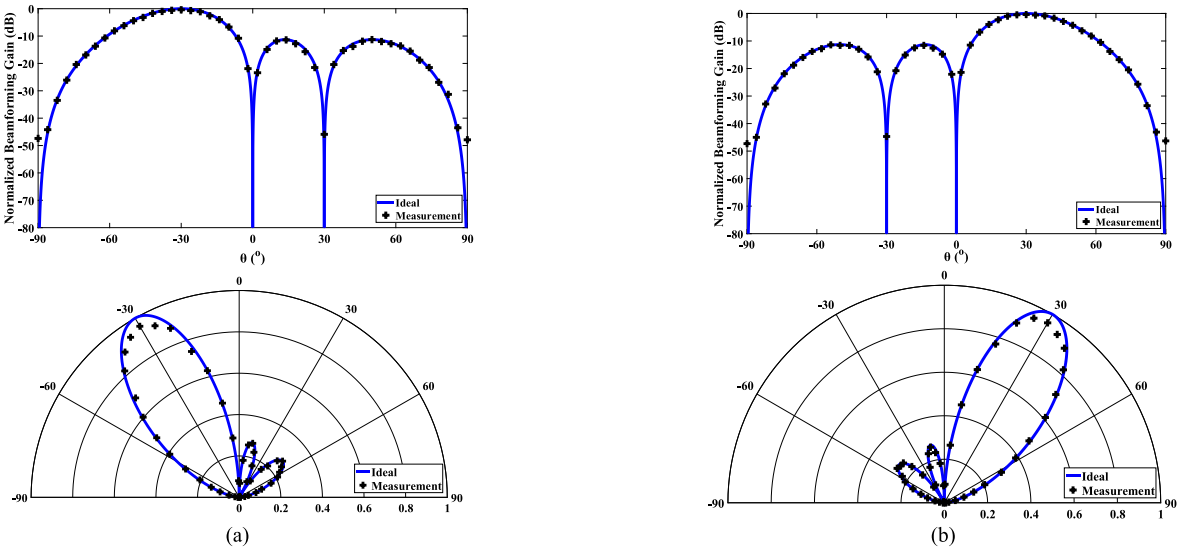

Fig. 15. Measured normalized beam pattern for: (a) $\theta = -30°$; (b) $\theta = 30°$.

(beam precision). The analog power consumption of the SCA, current references, and source follower drivers is 3 mW from 1.0 V supply.

Measured beamforming gain is plotted in Fig. 14(a) over 100 MHz bandwidth for $\theta = 0°$ for a swept CW signal. This plot shows that the beamforming gain is frequency independent and uniform, achieving >11.2 dB gain for the proposed 4-element delay-compensating beamformer. The gain deviation from ideal ($=$ 12 dB) is less than 0.8 dB for the entire 100 MHz bandwidth. Fig. 14(b) shows the spectrum capture for a 80 MHz BW signal at $\theta = 0°$. Again, a uniform beamforming gain of $\sim$12 dB is achieved. Fig. 15 shows the normalized beam patterns for two different AoA ($\theta = -30°$, $30°$) at two different single-tone frequencies. It can be seen that the measurement results follow the ideal beam pattern very closely for these two cases. In this measurement, the beamforming gain is measured for a fixed value of the TTD, by sweeping the AoA. The fabricated beamformer achieves a 4.6% error vector modulation (EVM) for a 4 Mb/s Quadrature Phase-Shift Keying (QPSK) signal in presence of a 12 dB stronger continuous-wave (CW) in-band interference signal. The constellation generated using a digital sampling oscilloscope (DSO) is shown in Fig. 16. The limited memory of DSO restricted our measurement to 4 Mb/s QPSK.

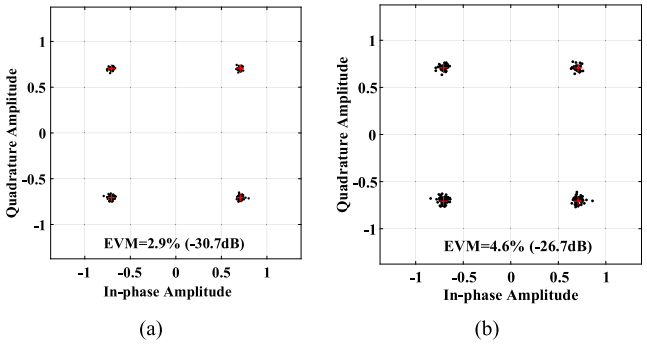

Fig. 16. Measured constellation for a 4Mb/s QPSK signal, (a) without blocker; and (b) in the presence of a 12 dB stronger CW in-band interference.

TABLE II compares the proposed delay-compensation element in a 4-element beamformer with the state-of-the-art. The discrete-time implementation achieves a wide range of 15 ns with 5 ps resolution enabling its application for larger arrays. Implementing the delay compensation in the BB improves the resolution and the range of the compensated delay demonstrating more than 3-bit improvement in range to resolution ratio. The proof-of-concept prototype developed in this work will be further extended to larger arrays as future work following

the design methodology in Section III. Future work will investigate the design of PI with lower power consumption and larger arrays with higher modulated bandwidths [25].

V. Conclusions

In this paper, a discrete-time delay-compensation technique has been developed for large array beamformers. A generalized design methodology is introduced that finds the optimal energy/area efficiencies for any given number of antenna elements, modulated bandwidth, ADC dynamic range, and PI resolution. The proposed delay-compensation technique is applicable to both an analog or hybrid beamformer. Trade-offs between analog, digital and hybrid delay-compensation beamformers are modeled using these parameters. Area- and energy-efficient discrete-time design techniques using switched-capacitor-based circuits are developed, avoiding the use of any area-hungry passive components. Compared to digital beamformers, the use of discrete-time delay-compensation through analog or hybrid beamforming helps in reducing the overall number of ADCs, while achieving precise beam resolution. A 4-element CMOS beamformer is demonstrated with frequency- uniform beamforming gain over 100 MHz modulated bandwidth. The proposed discrete-time technique achieves one of the largest delay range of 15 ns achieving a range/resolution ratio greater than 11.5 bit.

Acknowledgements

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