Four-Element Wide Modulated Bandwidth MIMO Receiver With >35-dB Interference Cancellation

Erfan Ghaderi, *Student Member, IEEE*, Ajith Sivadhasan Ramani, *Member, IEEE*, Arya A. Rahimi, *Student Member, IEEE*, Deukhyoun Heo, *Senior Member, IEEE*, Sudip Shekhar, *Senior Member, IEEE*, and Subhanshu Gupta, *Senior Member, IEEE*

***Abstract*— Active control of interference is necessary with increased cell density, more complicated environmental reflections, and coexistence of multiple networks for next-generation wireless communications. The existing radio receiver architectures for spatial interference cancellation (SpICa) are limited by the spatial nulls created by a phased-antenna array (PAA) and cannot cover wide modulated bandwidths (BWs). We propose a discrete-time-delay-compensating technique for canceling spatial interferences with wide modulated BWs to reduce the dynamic range requirement for the data converter. Integral to the proposed circuit is a switched-capacitor-based multiply-and-accumulate processor that incorporates a reconfigurable phase interpolator and time interleaver for precise digitally tunable delays and multiplication of the input signal to an orthogonal matrix. The digital time interleaver enables 5-ps resolution with a reconfigurable range up to 15 ns. The measured results demonstrate greater than 35-dB SpICa over 80-MHz modulated BWs in the 65-nm CMOS with 52 mW of power consumption.**

***Index Terms*— Discrete-time-delay (TD)-compensating, multiple-input multiple-output (MIMO) receiver array, spatial interference cancellation (SpICa), truncated Hadamard matrix, wide modulated bandwidth (BW).**

I. Introduction

FUTURE generations of wireless communication network demand addressing a completely new set of challenges including wider bandwidths (BWs), larger antenna array sizes, and higher cell density [1]. As next-generation sub-6-GHz and millimeter-wave (mmWave) networks [2] evolve, the dramatic shortening of intercell distances, coexistence of multiple networks, and complicated environmental reflections can significantly degrade the performance of radios without any spatial interference cancellation (SpICa).

Manuscript received November 15, 2019; revised January 30, 2020 and March 17, 2020; accepted March 26, 2020. Date of publication April 23, 2020; date of current version September 2, 2020. This work was supported in part by the National Science Foundation (NSF) CAREER under Award 1944688 and Award 1705026 and in part by the Natural Sciences and Engineering Research Council of Canada (NSERC). *(Corresponding author: Subhanshu Gupta.)*

Erfan Ghaderi, Arya A. Rahimi, Deukhyoun Heo, and Subhanshu Gupta are with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99163 USA (e-mail: erfan.ghaderi@wsu.edu; sgupta@eecs.wsu.edu).

Ajith Sivadhasan Ramani and Sudip Shekhar are with the Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC V6T1Z4, Canada.

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2020.2986441

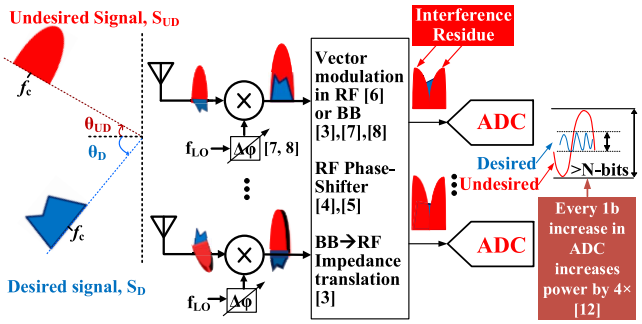

Fig. 1. PAA-based SpICa (implemented using vector modulation technique) causes leakage and requires higher dynamic range ADC for wide modulated BW interferers.

We consider in-band interference signals from transmitters of neighboring cells. Strong interferers degrade signal-to-interference-plus-noise ratio (SINR) for the signal of interest and effectively limit successful decoding of the desired stream due to the reduced number of quantization bits. Antenna arrays allow spatial filtering of interference regardless of the temporal and spectral characteristics of the interfering signal. However, mitigating wideband interference with analog arrays brings new challenges. As shown in Fig. 1, the state-of-the-art PAA-based array [3]–[10] has limited rejection capability toward wideband interference, because the variation in array response of different frequency components makes it hard to steer a deep null toward interference. In other words, the phase shift (PS) method used for interference cancellation in prior arts, approximating a time-delay (TD), cancels the interference at a single frequency, f. For next-generation systems with wide modulated BWs, it results in interference leakage and significantly higher dynamic range requirements for the baseband (BB) and the analog-to-digital converter (ADC) [11]. Fig. 1 shows that the received signals arephase-shifted and properly added to cancel the undesired signal. If Δt_{D} ($\Delta\varphi_{\mathrm{D}}$) and Δt_{UD} ($\Delta\varphi_{\mathrm{UD}}$) are the interelement delays (PSs) for the desired and undesired signals, respectively, mathematically, each antenna input is multiplied by $e^{j(i-1)\Delta\varphi_{\mathrm{UD}}}$, resulting in the overall phase for the undesired signal as $\Delta\varphi_{\mathrm{UD}} - 2\pi f \Delta t_{\mathrm{UD}}$. This term is frequency-dependent and zeroes at a single frequency only, leaving a residue for other frequencies at an offset from the carrier frequency, f_{C}. This residue leads to interference leakage causing increased dynamic range

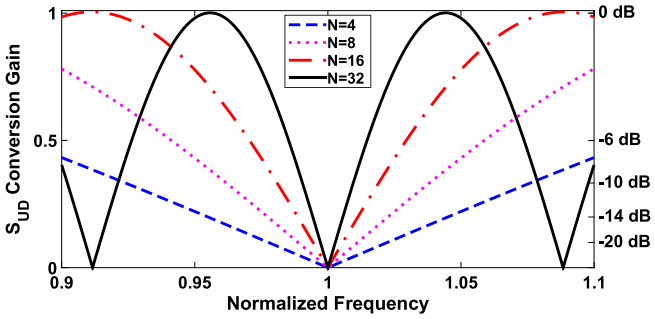

Fig. 2. SpICa simulation in a PS-based scheme versus normalized frequency over 20% fractional BW with different number of antennas.

requirement for the BB and ADC and consequently higher data conversion power consumption [12].

We study interference leakage in a PAA-based SpICa with 4, 8, 16, and 32 elements. Fig. 2 shows the rejection performance of the undesired signal across the normalized frequency with angle of arrival (AoA) $= 45°$. As it can be seen, for higher number of antennas, the undesired signal leakage is larger (higher conversion gain for S_{UD}) and cancellation starts to degrade even in narrower BWs. This simulation shows the need for a true-time-delay (TTD) implementation to compensate the delay between the received signals before performing SpICa.

In [3], a SpICa receiver (RX) is demonstrated using BB-to-RF impedance translation that models an inverse function of the incoming array pattern (four-element only). Although capable of single-tone SpICa when swept over 320 MHz, SpICa for modulated interferer is not demonstrated. Also, a cancellation BW of 320 MHz is obtained only at AoA $= 0°$, a case with no TD between the received signals and zero error between the TTD approximation with a PS element. An autonomous spatial filter for wide modulated SpICa at mmWave is implemented in [4] and [5]. However, its PS-based method introduces frequency-dependent filtering for applications at lower carrier frequencies due to large fractional BWs. Other techniques include switched-capacitor vector-modulation-based PS [7], local oscillator (LO), and BB PS [8], but high SpICa is achieved only for narrowband (NB) interferers. In [8], frequency-dependent and low SpICa ($\sim$18 dB) is also demonstrated for a 47-MHz modulated interference with 64-QAM modulation and 2% modulated signal fractional BW at 2-GHz carrier frequency.

The PS-based approximation (and hence, leakage) can be corrected by augmenting the RX front-end (FE) with a TTD in BB as described in Section II. However, such an approach needs precise delay generation or compensation. RF TTD implementation using *LC* or transmission line elements suffer from large area and insertion loss [13]. Digital TTD elements [14] implemented in post-ADC provide the most flexibility but at the cost of large ADC dynamic range in the absence of any SpICa technique. In [14], the digital implementation for a 16-element TTD with 16 oversampled ADCs consumes 453 mW (16 mW per ADC, 12.3 mW per element for digital TTD beamforming) for 100-MHz modulated BW. Also, Aurangozeb *et al.* [15] report 40-mW power consumption (only including ADCs) for a four-element digital RX array indicating power consumption constraints in the digital RX arrays.

In a downconversion RX, RF TD implementation is mathematically identical to TD introduced in LO together with BB [14], [16], [17]. The TD element in LO, operating at a single frequency, is simply analogous to a PS. After time-aligning the undesired signals at the BB, SpICa can be performed through subtracting half of the signals from the other half. After the subtraction, the undesired signal component is uniformly rejected across modulated BW without any residue compared with the PS-based SpICa, that is, the proposed approach is angle- and frequency-independent. In other words, a BB delay implementation can remove the frequency-dependent residue phase ($\Delta\varphi_{\mathrm{UD}} - 2\pi f \Delta t_{\mathrm{UD}}$) that exists in a PS-based SpICa scheme. Consequently, augmenting this PS in LO with a BB TD element can compensate the delay between the received signals, which is the proposed implementation in this work.

In our prior work [17], we introduced a high range-to-resolution ratio BB TTD for frequency-uniform beamforming gain to overcome the beam squinting problem in PS-based beamformers. This work introduces a BB delay-compensating technique with truncated Hadamard transform (THM) to implement a four-element TTD-based SpICa for wide modulated BW RX arrays. Our contributions in this article compared with our previous work [17] are as follows.

1) A wide modulated BW SpICa through THM and delay-compensating technique is developed (Sections II-A and II-C).
2) RF-FE design considerations and requirements for BB TTD implementation are presented and compared with RF TTD implementations (Section II-B).
3) Detailed transistor-level circuit implementation of the delay-compensating technique with integrated THM is described for the proposed TTD SpICa (Section III).
4) SpICa measurements that demonstrate performance for a four-element proof-of-concept prototype are presented (Section IV).

Section II presents the system design considerations for the proposed TTD-based SpICa in a wide modulated BW RF-FE. Section III describes the design of the proposed time-interleaved staggered switched-capacitor array implementing discrete TD-based SpICa. Section IV details the measured results for a four-element BB RX array. Section V concludes this article.

II. Proposed Delay-Compensating SpICa RX and System Design Considerations

A. Proposed SpICa RX for Wide Modulated BWs

In Fig. 3, the proposed BB TTD implementation for a four-element SpICa RX is shown. In this four-element array, there are six combinations of the elements that can perform SpICa (choosing two elements to be subtracted from the other two, $(4/2) = 6$). However, these six combinations are not all orthogonal to each other and they do not result in distinctive combinations of the elements (i.e., subtracting the first two elements from the last two is not distinctive from

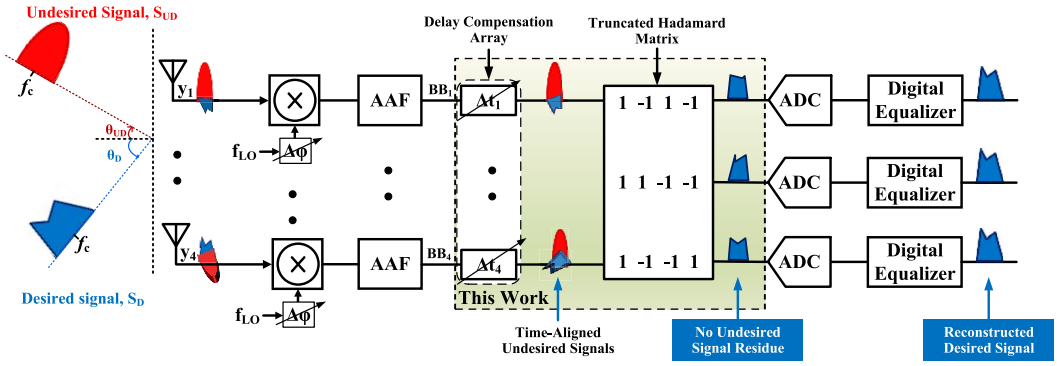

Fig. 3. Proposed discrete TD scheme with THM for wide modulated BW SpICa [antialiasing filter (AAF)].

TABLE I
RF-FE REQUIREMENTS AND APPLICATION REVIEW FOR THE PROPOSED TTD-BASED SPICA

Application	f_C (GHz)	BW (MHz)	Norm. Freq. Range	N	RF-FE Requirements for 40 dB SpICa		S_{UD} Max Conversion Gain in PS-Based SpICa (dB)	Proposed Implementation Requirements				RF TTD Implementation Requirements
					ε_{Gain} (%)	ε_{Phase} (°)		Δt_{UD} Inter-element Range (ps)	Overall Range $(N\text{-}1)\cdot\Delta t_{UD}$ (ps)	$\Delta\varphi_{UD}$ Resolution for 40 dB SpICa (°)	**Δt_{UD} Resolution for 40 dB SpICa (ps) $\varepsilon_{BB\text{-}TTD}$**	**Δt_{UD} Resolution for 40 dB SpICa (ps) $\varepsilon_{RF\text{-}TTD}$**
802.11ay	60	8640	0.93-1.07	4	2.1	1.2	-7.1	8.3	25	1.2	**0.40**	**0.05**
802.11ac	5	160	0.98-1.02	8	1.5	0.9	-14.0	100.0	700	0.9	**15.17**	**0.48**
5G NR n261	28	800	0.99-1.01	16	1.1	0.6	-9.1	17.9	268	0.6	**2.15**	**0.06**
5G NR n71	0.6	20	0.98-1.02	32	0.8	0.4	-5.1	833.3	25833	0.4	**60.97**	**2.00**

subtracting the last two from the first two). From the overall six combinations, there are three unique combinations of the time-aligned BB signals to perform SpICa. These three unique combinations construct a 4×3 matrix with only $+1$ and -1 entries, which forms a THM [18]. The received signals, including both desired and undesired, at the antenna are downconverted, phase shifted, and then fed to BB to perform TTD and SpICa. The proposed BB wide modulated BW SpICa solution comprises two main blocks: 1) the delay compensation array and 2) the cancellation matrix, which in this case is THM. The delay compensation array is implemented through a nonuniform discrete TD technique described further. The THM entries are simply constructed through differential implementation and the row's addition is done through charge-domain summation. The proposed solution, as shown in Fig. 3, implements a TTD-based SpICa over 100-MHz modulated BW in BB. A delay range of 15 ns (between the first and the last antennas) and a delay compensation resolution of 5 ps are chosen for our proof-of-concept four-element prototype. The 15-ns range with a 5-ps resolution allows realization of TTD-based SpICa for multiple applications as shown next.

B. RF-FE Design Requirements

Because the SpICa is being done at BB, the RF-FE must have sufficient linearity to downconvert the strong undesired signal without distorting the desired signal, similar to requirements in prior-art BB SpICa [4], [8]. Mixer-first receivers can relax the RF-FE linearity requirements [7], [19], and this will be explored in our future work. Further RF-FE impairments, especially amplitude and phase mismatches between the elements, must be taken into design considerations so as to not limit the performance of BB SpICa techniques. The RF-FE impairments can be modeled as gain and phase errors in the ith RF-FE transfer function characteristics from y_i to BB_i in Fig. 3 (a conventional RF-FE has been added for illustration only). These errors impair the RF-FE conversion gain ($G_{RF\text{-}FE}$) as in the following equation:

$$G_{RF\text{-}FE} = G \cdot (1 + \varepsilon_{Gain}) \cdot e^{j(\varepsilon_{Phase})} \tag{1}$$

where G is the ideal RF-FE conversion gain, ε_{Gain} is the RF-FE gain error, and ε_{Phase} is the RF-FE phase error. Table I uses the above expression to derive RF-FE design requirements for SpICa for four different applications spanning both sub-6-GHz and mmWave frequency bands. For this calculation, we assume that the even elements are subtracted from the odd elements and we find the maximum gain or phase error that results in 40-dB SpICa. For calculation of gain error, we assume the phase error to be zero, and vice versa. The number of elements (N) and the desired SpICa performance place an upper limit for both ε_{Gain} and ε_{Phase}. It can be observed from Table I that these errors are inversely proportional to $\sqrt{N}$ (Appendix B). Note that if the gain errors and the phase errors of the elements are independent random variables, no matter which half is subtracted from the other half, on average the

SpICa will be the same. Thus, the calculations in Table I are not limited to the case where the even elements are subtracted from the odd elements.

For the scenarios described in Table I, PS-based SpICa results in imperfect cancellation and interference leakage. This leakage is quantified by S_{UD} max conversion gain in Table I (also illustrated in Fig. 2). A higher decibel value signifies larger interference leakage. The presented results here indicate that TTD-based SpICa is needed to avoid interference leakage.

Table I also shows the required interelement TTD range (maximum interelement delay, which in a RX with $\lambda/2$ antenna spacing is equal to $1/2f_{\mathrm{C}}$ [17]), overall TTD range, LO phase shifter ($\Delta\varphi_{\mathrm{UD}}$) resolution, and TTD resolution for different applications for the proposed TTD-based SpICa (Fig. 3). Clearly, the PS resolution for 40 dB of SpICa is equal to the phase error ($\varepsilon_{\mathrm{Phase}}$) for 40 dB.

Finally, the TTD resolution in the proposed BB implementation is also compared with the TTD implementation only at RF. The finite resolution is modeled as an error in the TTD element and the nonideal SpICa based on this error is calculated using the following expressions:

$$\mathrm{SpICa}_{\mathrm{RF\text{-}TTD}} = \sum_{\mathrm{i}=1}^{N} (-1)^i \cdot e^{j2\pi \cdot f_{\mathrm{RF}} \cdot \varepsilon_{\mathrm{RF\text{-}TTD}}(i)} \quad -f_{\mathrm{C}}\frac{\mathrm{BW}}{2} \le f_{\mathrm{RF}} \le f_{\mathrm{C}} + \frac{\mathrm{BW}}{2} \tag{2}$$

$$\mathrm{SpICa}_{\mathrm{BB\text{-}TTD}} = \sum_{i=1}^{N} (1)^i \cdot e^{j2\pi \cdot f_{\mathrm{BB}} \cdot \varepsilon_{\mathrm{BB\text{-}TTD}}(i)} 0 \le f_{\mathrm{BB}} \le \mathrm{BW} \tag{3}$$

where $\varepsilon_{\mathrm{RF\text{-}TTD}}(i)$ and $\varepsilon_{\mathrm{BB\text{-}TTD}}(i)$ represent the ith TTD element resolution in the RF TTD and the proposed implementation, respectively. We consider a generic case for calculating the SpICa where the even elements are subtracted from the odd elements. Conceptually, the BB TTD resolution requirement is inversely proportional to the modulated BW. This offers a significant relaxation in the design of the BB clock circuitry (presented further in Section III) when compared with RF TTD implementation where the TTD resolution is inversely proportional to carrier frequency. These requirements are also reported in Table I for four different applications. For example, the PS-based SpICa in a 32-element RX for 5G NR n71 band results in high interference leakage (undesired signal conversion gain as high as -5.1 dB). To solve this interference leakage problem through RF TTD implementation and for SpICa of 40 dB, the power/area hungry TTD elements at RF are needed with resolution of $\sim$2 ps and overall range of $\sim$25.8 ns, resulting in effective number of bits (ENOB) of 13.7 bits. However, in our proposed implementation, the resolution of the TTD element is relaxed to $\sim$61 ps, resulting in $\sim$5-bit reduction in the TTD element's ENOB. The overall range and the resolution of the TTD elements in the proposed implementation for four applications shown in Table I show the need for a high range, high precision, and scalable BB TTD implementation.

Section II-C presents the delay-compensating technique that has been used in the proposed implementation to realize the range, resolution, and scalability requirements desired from the TTD elements.

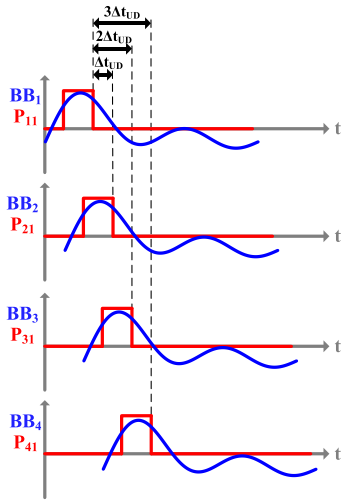

Fig. 4. Offset-sampling technique used to implement TD.

C. Offset-Sampling for Delay-Compensating

Fig. 4 shows the offset-sampling technique used to implement the discrete TD array and compensate the undesired TD between BB signals. Intuitively, sampling the BB signals with time-delayed clocks is equivalent to sampling the time-delayed version of those signals with the same clock. Using this discrete TD technique, the BB delay compensation array is realized. The resolution of the delay-compensation elements, which in this discrete TD structure is determined by the resolution of the delay between the sampling clocks, determines the SpICa performance.

Note that in Fig. 4, the longest delay sets the required level of interleaving. For example, if eight elements are implemented, the delay between the first and the last antennas increases to 35 ns (assuming 5 ns between two elements). To compensate this new total delay, we implement multilevel interleaving in the clock-generation unit in the BB. Thus, instead of changing the sampling rate that is determined by the signal BW, we scale the level of interleaving to 8. By doing so, there will be eight sets of sampling phases and each set consists of eight interleaved phases. This results in a design that is highly scalable in terms of array size, SpICa performance, and signal BW as described in Section III. For higher number of elements ($N \gg 4$), hybrid structure can be used [17], where the array is divided into subarrays and partial SpICa is performed on each subarray.

III. Proposed Discrete TD-Based SpICa Circuit Design

A. THM Implementation Through Time-Interleaved Switched Capacitor Sampling

In Fig. 5, an analog implementation of the THM is proposed. In this structure, each row of the THM is implemented as an analog multiply-and-accumulate (MAC), with four multipliers ($M_1 \ldots M_4$) and one accumulator. Differential

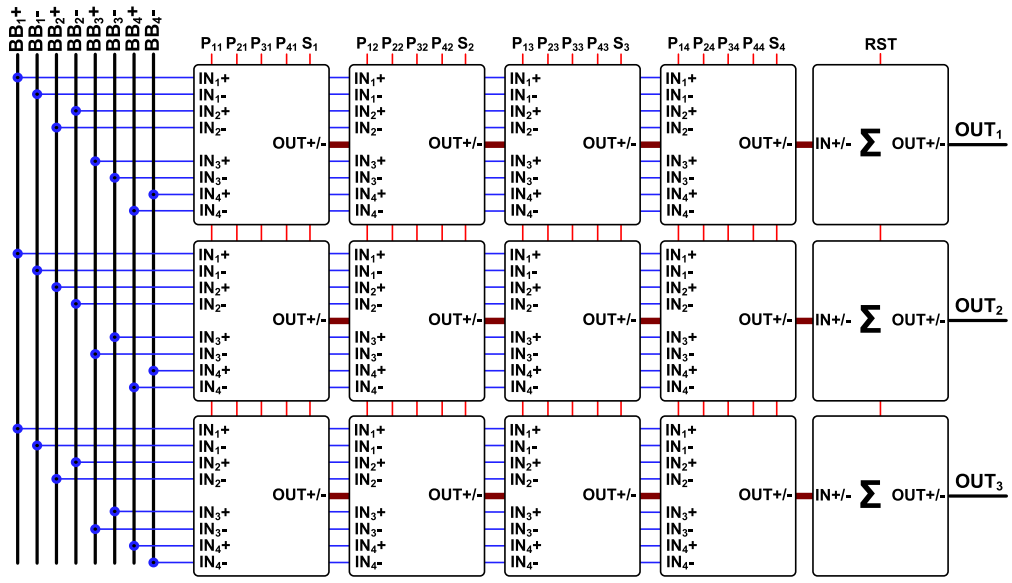

Fig. 5. THM realization through differential analog MAC implementation.

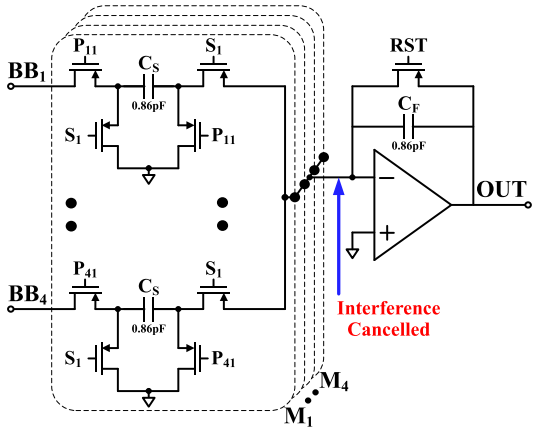

Fig. 6. Simplified single-ended representation of THM rows' implementation. Note that the interference cancellation is done at the virtual ground resulting in significantly relaxed linearity requirements.

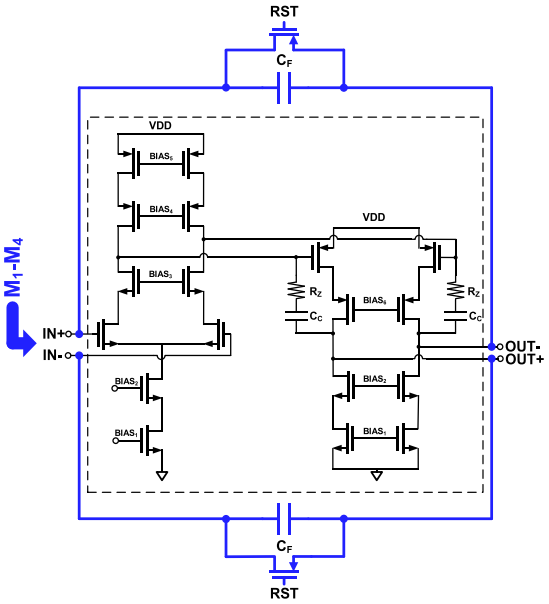

Fig. 7. Two-stage internally compensated OTA with the feedback network (bias circuits are not shown).

implementation is used to simplify THM entries' realization. By simply flipping the polarity of the corresponding inputs to -1, the THM can be realized without any extra hardware requirements. Multiplications are achieved using the conventional bottom-plate sampling switched-capacitor circuit and accumulation is achieved using a fully differential operational transconductance amplifier (OTA)-based parasitic-insensitive summer (Fig. 6). Each accumulator sums the inputs, delayed and sampled on the four capacitors during the SUM phases ($S_1 \ldots S_4$). This switched-capacitor-based implementation of a BB RX requires four phases for sampling ($P_{1i}, \ldots, P_{4i}$) followed by summation (S_i) and reset (RST) phase, in a four-element array (clock-generation unit discussed in Section III-B).

During each sampling phase ($P_{1i}, \ldots, P_{4i}$), the input signal from each RX is sampled on a sampling capacitor (C_S). The input sampler is implemented using a PMOS switch optimized to provide the maximum linearity to handle input signals between 0.4 and 1 V. The value of C_S is determined by the noise requirements of the RX. After the last sampling phase (P_{4i}), the stored charges on each capacitor are shared in the S_i phase. This charge sharing performs an averaging function. To change this functionality to summation, the shared charges are transferred to the feedback capacitor (C_F) in a switched-capacitor summer. The OTA used in this adder must satisfy SNR and signal BW requirements of the RX. In the summation phase, there is a feedback network on the OTA, with feedback coefficient of 1/4 (consisting of four effective sampling capacitors and one feedback capacitor). Considering these requirements, the OTA is implemented as a two-stage internally compensated structure with Miller compensation (Fig. 7). The OTA is designed with more than 70-dB open-loop gain, 685-MHz unity-gain BW, and 72° phase margin.

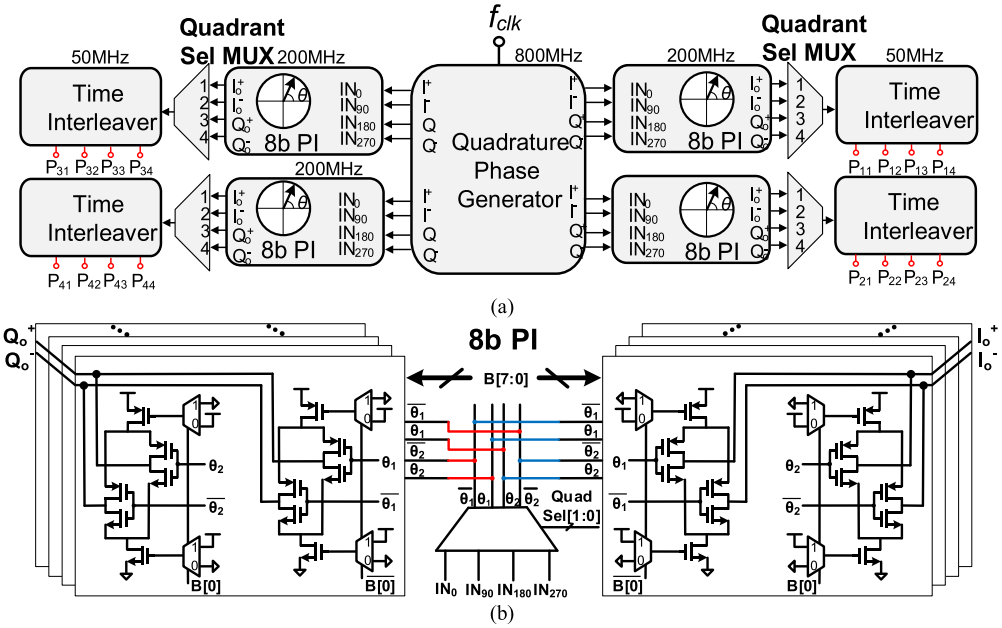

Fig. 8. (a) Time-interleaver topology with 5-ns delay between consecutive antennas and 5-ps resolution. (b) 8-bit quadrature PI schematic.

These values ensure that the desired cancellation performance is met across the process, voltage and temperature (PVT) variations. Because the input nodes of the OTA do not vary significantly (virtual ground) and the output nodes just carry the weaker desired signals (the undesired has been rejected), telescopic cascode structure has been used for both stages. A wide-swing cascode current mirror is used that mirrors the input off-chip bias current (=200 μA) to each of the three OTAs consuming 2 mA at 1-V supply. The BW of the common-mode feedback loop is set to be greater than the Nyquist frequency to allow first-order rejection of common-mode noise and interference. Note that the interference cancellation happens prior to summation resulting in significantly reduced linearity requirements for the summer.

Implementations supporting gigahertz BW can be realized through OTAs with higher unity-gain-BW. However, this requires further research into appropriate OTA topology and a conventional folded-cascode or telescopic amplifier will not be sufficient. The binary ($\pm$1) entries in the proposed THM-based MACs permit: 1) half of the signal vector to be uniquely combined with the other half; 2) easy realization through differential implementation without requiring any extra hardware; and 3) easy scalability to a higher number of elements thus promising low-latency operation. A low-power source-follower buffer consuming 0.25 mA is used to drive each MAC output (OUT) for off-chip measurement.

B. Clock-Generation Circuit Implementation

Fig. 8(a) shows the proposed time-interleaver topology. For our proof-of-concept prototype, keeping in mind the limitations of our measurement setup for a maximum BW of 100 MHz and four elements, we choose a precision of 5 ps and a maximum range of 15 ns (deliberately larger than needed) between the first and the last antennas, in the sampling clock phases. The time-interleaver resolution determines the theoretical maximum interference rejection. In the proposed design, Nyquist sampling results in a sampling clock frequency of 200 MHz (twice of BB BW, 2×100 MHz). The external 800-MHz single-phase clock (f_{clk}) is first terminated with a 50-Ω on-chip resistor and is fed to a quadrature-phase generator circuit [20] after amplification to rail-to-rail swing. The quadrature-phase generator provides quadrature outputs (I^-, I^+, Q^-, Q^+) at 200 MHz with complete cycle coverage (=360°) and period of $T_S = 5$ ns. These quadrature phases are fed to an 8-bit-binary digital quadrature-phase interpolator (PI) [21] which is capable of 5-ps resolution (=1.25 ns/256) and has a maximum 5-ns range after the four differential quadrature outputs of the PI (I_o^-, I_o^+, Q_o^-, Q_o^+) are selected by the MUX. Both the PI and MUX are programmed using an on-chip serial-to-parallel (SPI).

The period of the 200-MHz clock is insufficient to cover the required time span of 15 ns between the first and the last antennas. This is remedied by generating four phases ($P_{11}, \ldots, P_{14}$), from each Q-MUX output, for each quadrant select MUX, at 50 MHz with a 12.5% ON-time from a time interleaver. These 16 phases ($P_{11}, \ldots, P_{44}$) provide the required staggered-time-interleaved clocks as shown in Fig. 9. A digital implementation with power consumption proportional to $C \cdot \text{VDD}^2 \cdot f_{\text{clk}}$ permits scaling with CMOS process, VDD, and BW. A finer resolution is preferred in improving the cancellation performance, but it also comes at the overhead of power and area in clocking. The resolution is chosen as 5 ps to show the scalability of this design in terms of SpICa performance. A range of 5 ns is chosen as a delay between each consecutive antenna, resulting in 15 ns of the overall range. Such a large range is again chosen to prove that this design can be used in larger arrays, where the delay between received signals at the first and the last antennas can be a large value.

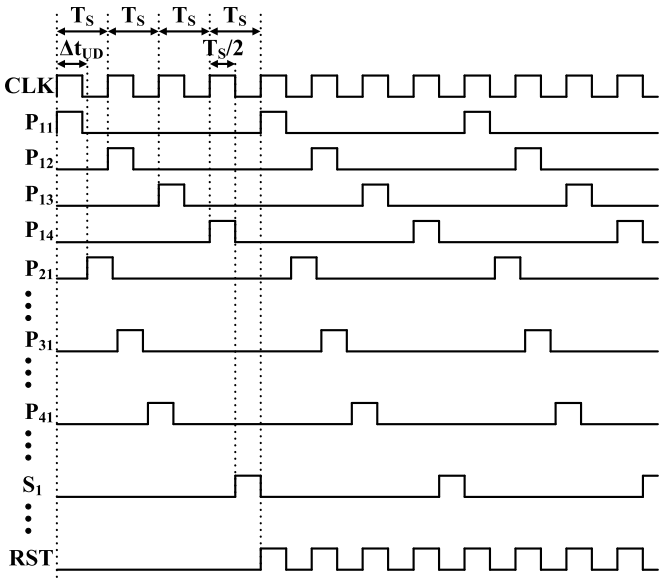

Fig. 9. Required phases to span 15-ns range and ensure proper functionality of the discrete TD-based SpICa implementation.

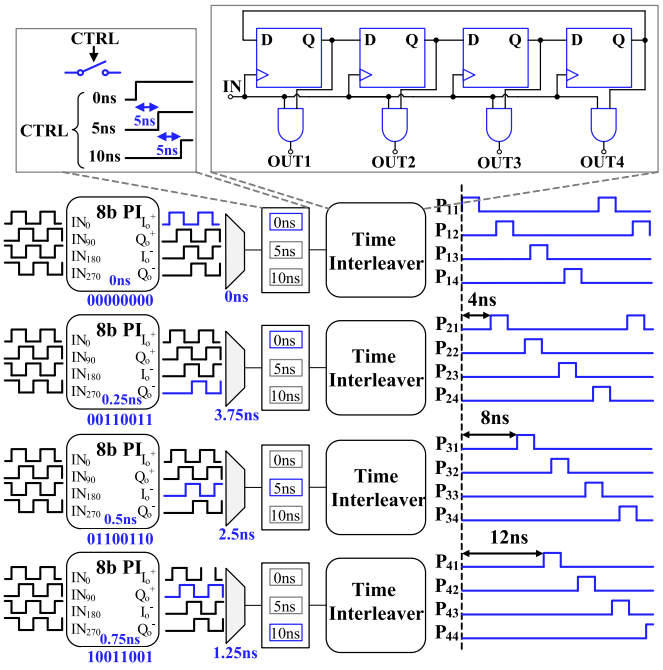

Fig. 10. States of the time interleaver and important phases for delay compensation of 4 ns between consecutive antennas.

In Fig. 10, the state of each PI and MUX is illustrated to generate a delay compensation of 4 ns between consecutive antennas. Each of the four PIs is configured independently using the SPI data bits. The first PI does not interpolate any of the phases generated by the quadrature-phase generator preceding the PI. As such, the I_o^+ phase is selected by the MUX and fed to the time interleaver to generate the first set of sampling phases ($P_{11}, \ldots, P_{14}$). These sampling phases are then applied to the first input signal (BB_1 in Fig. 5). To generate 4 ns of delay for the second antenna element, the second PI interpolates the input clocks by 0.25 ns. Selecting the Q_o^- phase of the PI by MUX results in 4-ns relative delay (0.25 ns from the PI and 3.75 ns from choosing the Q_o^- phase). To generate 8 ns of delay for the third antenna element, the third PI interpolates the input clocks by 0.5 ns. Selecting the I_o^- phase of the PI by MUX results in 3-ns relative delay (0.5 ns from the PI and 2.5 ns from choosing the I_o^- phase). Another 5 ns ($= T_S$) of the desired relative delay is introduced by enabling the time interleaver only after 5 ns relative to the first two time interleavers. This relative delay can only be controlled as 0, T_S, or $2T_S$, in our implementation. Finally, a delay of 12 ns is implemented for the fourth antenna element.

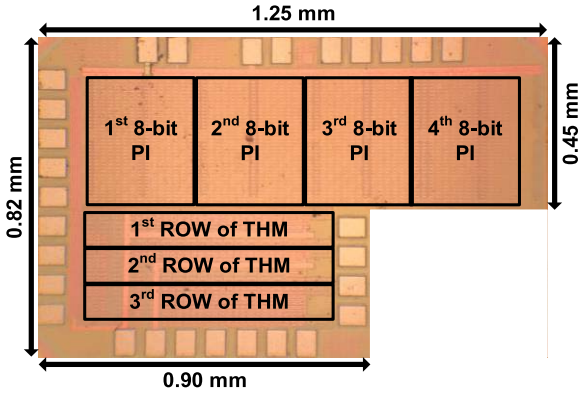

Fig. 11. Die micrograph in the 65-nm CMOS.

IV. Measurement Results

The four-element multiple-input multiple-output (MIMO) BB RX has been implemented in a 65-nm CMOS process in an area of 0.65 and 0.9 mm^2 without and with pads, respectively, as shown in Fig. 11. The prototype is packaged in a Quad-Flat Package (QFP) enclosure to minimize parasitic bond wires. An SPI control port is used to set the on-chip digital phase interpolation and time interleaving. The delays between the RX antenna signals are implemented through two National Instruments (NI) PXIe-5450 arbitrary waveform generators (AWGs) with four differential outputs and 145-MHz modulation BW as shown in the test setup in Fig. 12. Both single-tone and modulated signals are applied as inputs to characterize the SpICa.

The gain mismatch between the channels degrades the SpICa performance, as described in Section II-B. To remove the SpICa degradation due to the mismatch between the channels in the fabricated chip, we first measured each channel's input-to-output characteristics by applying a constant amplitude signal to each input (one at a time) and measuring the output amplitude. The gain mismatch between the channels is then calibrated by equalizing each input amplitude through the initial input-to-output gain measurement.

Fig. 13 shows the measured SpICa performance for multiple AoA_{UD} (12°, 24°, and 53° corresponding to $\Delta t_{UD} = 1$, 2, and 4 ns) and a swept single tone from 1 (balun-limited) to 99 MHz. As it can be seen, the cancellation across the entire band is independent of AoA and >46 dB is achieved with 1.5× improvement in fractional BW over prior art [3].

Fig. 14(a) shows the measured wide modulated BW SpICa performance for 80-MHz BW at the output of the THM's second row with one input (no cancellation) and four inputs

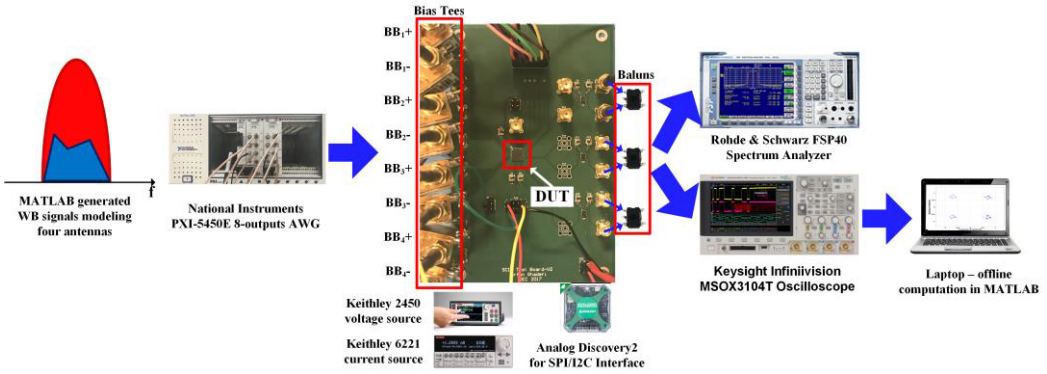

Fig. 12. Test setup.

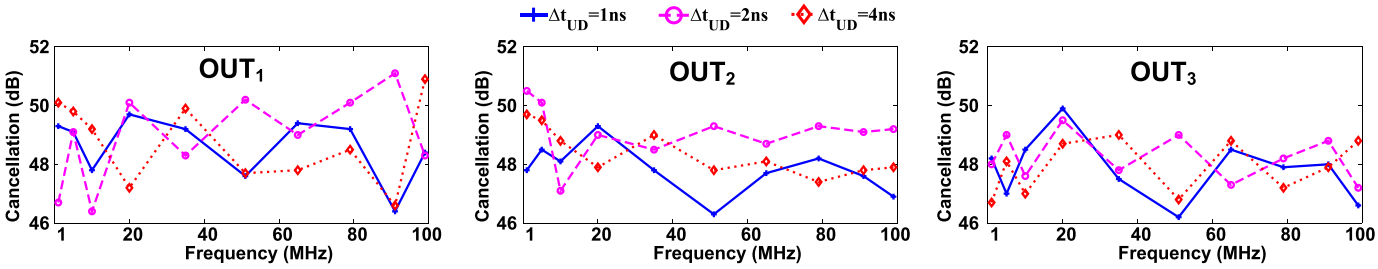

Fig. 13. Measurement results of the single-tone undesired signal SpICa performance versus frequency for three cases of Δt_{UD}.

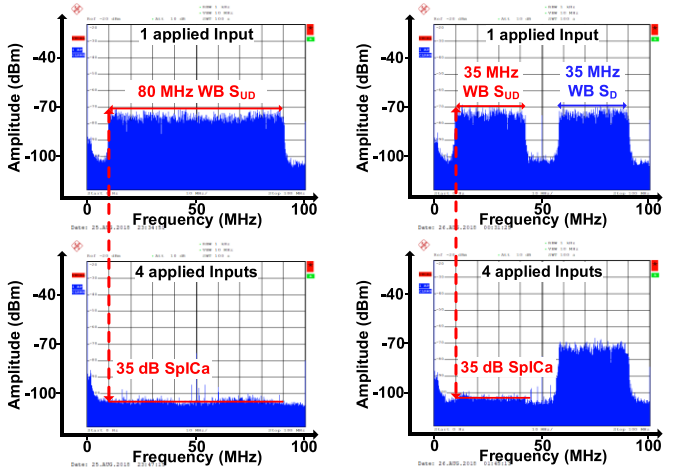

Fig. 14. SpICa measurement for a wide modulated BW undesired signal versus frequency. (a) Without any desired signal. (b) With a wide modulated BW desired signal.

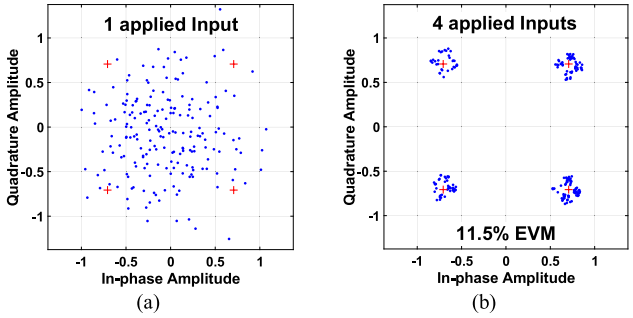

Fig. 15. Measured constellation of a desired 4-Mb/s QPSK signal in the presence of a 12-dB stronger wide modulated BW interference. (a) One applied input (without SpICa). (b) Four applied inputs (with SpICa).

TABLE II
PERFORMANCE SUMMARY

Technology (nm)	CMOS 65
VDD (V)	1.0
Power Consumption (mW)	Analog = 8 Clock 44 Total = 52
Area (mm^2)	0.9
P_{IN1dB} (dBm)	4.7
P_{IIP3} (dBm)	10.6
Output Referred Noise (μV_{rms})	330

(cancellation enabled), demonstrating >35-dB SpICa for a fractional BW of 80% in the dc-100-MHz band (80 MHz is selected to visualize the plot easier and demonstrate the SpICa clearly). Similar performance is obtained when the cancellation is performed with other THM rows, confirming that the proposed architecture can be used for generating multiple versions of the desired signal simultaneously, while canceling the undesired interference signals.

Fig. 14(b) shows the desired- and the undesired-signal spectrum (35 MHz within the dc-100-MHz band) with one and four inputs. In this measurement, $\mathrm{AoA_{UD}} = 90°$ and $\mathrm{AoA_D} = 45°$. More than 35-dB SpICa across the entire BW of the undesired signal is obtained again. Note that the BW of the desired and the undesired signal is reduced from 80 to 35 MHz to visually show the cancellation on a 100-MHz plot.

Fig. 15 depicts SpICa performance for a wide modulated BW [40-Mb/s quadrature phase-shift keying (QPSK)]

TABLE III
COMPARISON TO PRIOR-ART SPATIAL CANCELLATION IMPLEMENTATIONS

		ISSCC2019 [4]	TMTT2019 [5]	RFIC2016 [6]	JSSC2017 [3]	TMTT2017 [8]	This Work
Implementation		RF only	RF only	RF only	RF+BB	RF+BB	**BB only**
# Elements		4 inputs/4 outputs	8 inputs/2 outputs	4 inputs/1 output	4 inputs/4 outputs	4 inputs/1 output	**4 inputs/3 outputs**
# Independent Interferences		3	2	1	3	1	**1**
Technology (nm)		CMOS SOI 45	BiCMOS SiGe130	CMOS 65	CMOS 65	CMOS 180	**CMOS 65**
Resolution		NR	NR	6-b I/Q	Phase: 6.5-b Amp: 3.9-b	Phase: 6-b Amp: 6-b	**8-b (5 ps) range: 15 ns**
Swept-SpICa[1]	**Cancellation (dB)**	50-62	41-54	32	51-56	NR	**46-51**
	Swept Range (MHz)	900[2]	700[2]	100[3,4]	320[3,4]	NR	**99[4]**
Modulated Signal SpICa	**Cancellation (dB)**	20[5]	23.5[6]	–	–	~18[7]	**>35**
	BW	500 MHz[8]	500 MHz[8]			47 MHz	**80 MHz**
	Fractional BW (%)	2	2			2	**3-9[9]**

[1]Swept interference f_C measurements, [2]Swept wideband SpICa, [3]20dB SpICa BW, [4]Swept CW interference [5]Visually derived from slide 35 of ISSCC 2019 presentation, [6]Derived from Fig.12, [7]Visually derived from Fig.30, [8]Raw bandwidth calculated for 3Gb/s 64-QAM, [9]For this number, the f_C is assumed between 915MHz and 2.4GHz.

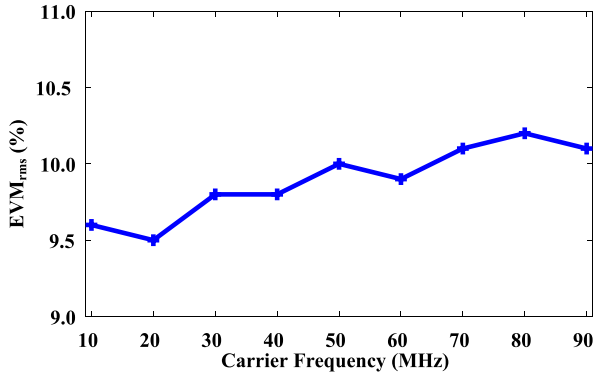

Fig. 16. Simulated EVM performance versus the desired signal carrier frequency.

interferer with AoA = 60° and 12 dB higher in power than the desired 4-Mb/s QPSK signal (AoA = 0°), with an offline-computed error vector magnitude (EVM) of 11.5%. The SpICa data are sampled and stored using the digital sampling oscilloscope followed by EVM estimation in MATLAB. Limited memory in the AWGs and sampling oscilloscope restricted our measurements to 4-Mb/s QPSK modulation only.

To further prove the wideband operation of the proposed work, the circuit is simulated for various carrier frequencies at 4 Mb/s of the desired signal, with $\text{AoA}_\text{D} = 0°$, and in the presence of a 12-dB stronger 40-Mb/s QPSK interference, with $\text{AoA}_\text{UD} = 60°$. The simulation result of the EVM performance versus the desired signal carrier frequency is plotted in Fig. 16. The negligible variation in EVM over the entire frequency range shows the wideband operation of the proposed implementation.

The measured total power consumption of the analog implementation of the THM is 8 mW/100 MHz. Another 44 mW is consumed in clocking including the 0.8–0.2 GHz quadrature-phase generator, the four 8-bit PIs, and the time-interleaving circuit. The clocking power can be decreased further to less than 5 mW for smaller resolutions (e.g., the clocking power is <5 mW for 4-bit resolution). Table II summarizes the performance of the implemented SpICa. The measured $P_{1\,\text{dB}}$ compression point of the BB RX is 4.7 dBm with 10.6-dBm third-order input intercept point (IIP3). The measured noise power at the THM output is 330 μVrms. Other phase interpolation techniques are currently being investigated to significantly reduce the power consumption for future prototypes [22], [23].

The clocking power can also be decreased if a reduced delay range is needed. The design constraints and power consumption associated with realization of a high-dynamic range ADC are thus significantly relaxed. With the demonstrated >35-dB wide modulated BW SpICa, the ADC dynamic range is significantly relaxed by nearly 6 bits. Notably, a 1-bit reduction in ADC resolution leads to nearly 4× power savings [12] for ADCs limited by thermal noise. In addition, the ADC power consumption can increase quadratically for high sampling frequencies as in [12].

Table III compares the proposed wide modulated BW SpICa with prior art. The demonstrated SpICa of >35 dB over 80 MHz of wide modulated BW interferers is independent of the carrier frequency. In fact, this BB RX can be augmented to any RF-FE with carrier frequencies as low as 100 MHz ($\Delta t_{\text{MAX}} = 1/2 f_C$). For typical applications in the frequency range of 915 MHz to 2.4 GHz, our BB RX results in fractional BW of 3%–9%, the highest modulated signal fractional BW compared with the prior arts. The delay range BW product for the proposed TTD implementation is 1.5 (=15 ns × 100 MHz).

Wide modulated BW interference cancellation is demonstrated in [8], where a 47-MHz 64-QAM signal is filtered in the presence of a desired 20-MHz 64-QAM signal, resulting in SpICa at 2% modulated signal fractional BW. Also, [4] and [5] show wide modulated SpICa for a 3-Gb/s 64-QAM signal at high carrier frequency of >26 GHz with cancellation <23.5 dB and 2% modulated signal fractional BW. In comparison, our work demonstrates a uniform cancellation of 80-MHz modulated BW.

V. CONCLUSION

This article successfully demonstrated a TTD-based spatial interference canceling technique for a four-element receiver array. We overcame the limited resolution of TTD elements

at RF for SpICa using discrete-time offset-sampling implementation at BB which considerably relaxed the required TTD resolution. An energy-efficient architecture is presented that uses discrete-TD-compensating technique with truncated Hadamard matrix (THM) to cancel in-band interferers spanning the entire modulated signal BW with large resolution and at the same time high energy efficiency. Measurements demonstrate 35-dB uniform undesired interference cancellation over 80 MHz and in the presence of desired signal. The proposed TTD-based SpICa for in-band modulated signals can augment the existing phased-array receiver FEs with high fractional BW, making it easy to adapt for even wider modulated BWs for next-generation communication links.

APPENDIX A
DESIRED SIGNAL CHARACTERIZATION IN THE PROPOSED SPICA

Since the TTD implementation at LO in conjunction with BB is mathematically identical to RF TTD implementation, we examine the effect of SpICa on the desired signal in the RF domain. Referring Fig. 3, at the output of the THM ($\mathrm{OUT}_i(t)$, $i = 1, 2, 3$), the undesired signal is eliminated and the residue signal (which is only a function of the desired signal) can be written as

$$\mathbf{OUT}(t) = \begin{bmatrix} \mathrm{OUT}_1(t) \\ \mathrm{OUT}_2(t) \\ \mathrm{OUT}_3(t) \end{bmatrix} = \begin{bmatrix} +1 & -1 & +1 & -1 \\ +1 & +1 & -1 & -1 \\ +1 & -1 & -1 & +1 \end{bmatrix} \begin{bmatrix} S_{\mathrm{D}}[t] \\ S_{\mathrm{D}}[t + (\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})] \\ S_{\mathrm{D}}[t + 2(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})] \\ S_{\mathrm{D}}[t + 3(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})] \end{bmatrix}. \tag{A1}$$

This equation can be rewritten in the frequency domain, as in (A2), and the desired signal conversion gain vector, $\mathbf{G_D}(j2\pi f)$, can be defined as (A3)

$$\mathbf{OUT}(j2\pi f) = \begin{bmatrix} \mathrm{OUT}_1(j2\pi f) \\ \mathrm{OUT}_2(j2\pi f) \\ \mathrm{OUT}_3(j2\pi f) \end{bmatrix} = \begin{bmatrix} +1 & -1 & +1 & -1 \\ +1 & +1 & -1 & -1 \\ +1 & -1 & -1 & +1 \end{bmatrix} \begin{bmatrix} S_{\mathrm{D}}(j2\pi f) \\ S_{\mathrm{D}}(j2\pi f) e^{j2\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} \\ S_{\mathrm{D}}(j2\pi f) e^{j4\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} \\ S_{\mathrm{D}}(j2\pi f) e^{j6\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} \end{bmatrix} \tag{A2}$$

$$\mathbf{G_D}(j2\pi f) = \frac{\mathbf{OUT}(j2\pi f)}{S_{\mathrm{D}}(j2\pi f)} = \begin{bmatrix} G_{\mathrm{D1}}(j2\pi f) \\ G_{\mathrm{D2}}(j2\pi f) \\ G_{\mathrm{D3}}(j2\pi f) \end{bmatrix} = \begin{bmatrix} 1 - e^{j2\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} + e^{j4\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} - e^{j6\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} \\ 1 + e^{j2\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} - e^{j4\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} - e^{j6\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} \\ 1 - e^{j2\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} - e^{j4\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} + e^{j6\pi f(\Delta t_{\mathrm{UD}} - \Delta t_{\mathrm{D}})} \end{bmatrix}. \tag{A3}$$

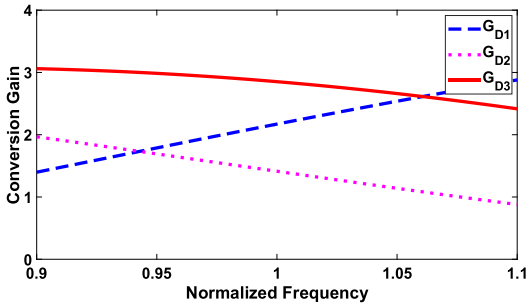

Fig. 17. Desired signal conversion gain versus normalized frequency over 20% fractional BW in the proposed SpICa scheme.

As seen in (A3), the desired signal is affected by a known frequency-dependent profile that can be equalized after digitization (Fig. 3). The transfer function profile for each of the signal paths in (A3) depends on the difference between the desired and undesired TD, which itself is a function of AoA of both desired and undesired signals. Fig. 17 plots these conversion gains versus normalized frequency, for a signal occupying a BW equivalent to 20% of the center frequency. In this simulation, for $\mathrm{AoA_D} = 0°$ and $\mathrm{AoA_{UD}} = 45°$, it can be seen that the conversion gains for almost the entire band are more than one and their frequency dependence profiles can be compensated by a digital equalizer post ADC or transmitter coding prior to communication.

APPENDIX B
GAIN AND PHASE ERROR EFFECTS ON THE SPICA PERFORMANCE IN AN N-ELEMENT ARRAY

In this section, we formulize the relationship between the array size and the effects of gain and phase error on SpICa performance. In the presence of gain and phase error, the SpICa residue can be written as

$$\mathrm{SpICa}_{\mathrm{Gain\&Phase}} = \sum_{i=1}^{N} (-1)^i \cdot G \cdot (1 + \varepsilon_{Gi}) \cdot e^{j\varepsilon_{Pi}} \tag{A4}$$

where G is the ideal gain of the RF-FE and ε_{Gi} and ε_{Pi} are the ith channel's gain and phase error, respectively. These errors can be modeled as random variables with mean of zero and bounded to $\pm\sigma_G$ and $\pm\sigma_P$.

Next, each error is individually analyzed to find a closed-form solution for the SpICa residue in the presence of gain or phase error. Considering only gain error

$$\mathrm{SpICa}_{\mathrm{Gain}} = \sum_{i=1}^{N} (-1)^i \cdot G \cdot (1 + \varepsilon_{Gi}) = G \cdot \sum_{i=1}^{N} (-1)^i \cdot (\varepsilon_{Gi}). \tag{A5}$$

This error is equal to the addition of N independent and identically distributed random variables, with mean of zero and variance of $(\sigma_G^2/3)$ (negative of ε_{Gi} is another random variable with the same properties). Hence

$$|\mathrm{SpICa}_{\mathrm{Gain}}| \propto \sqrt{N} \cdot \sigma_G. \tag{A6}$$

The result in (A6) shows that for a constant SpICa performance (e.g., 40 dB mentioned in Section II-B), the required error will be inversely proportional to $\sqrt{N}$.

A similar analysis is performed considering only phase error as follows:

$$\mathrm{SpICa}_{\mathrm{Phase}} = \sum_{i=1}^{N} (-1)^i \cdot G \cdot e^{j\varepsilon_{Pi}}. \tag{A7}$$

Taking advantage of the discussions in [24] about the effect of phase error in beamformers and adapting the same methodology to our SpICa implementation, we can simplify the SpICa residue caused by the phase error to

$$|\mathrm{SpICa}_{\mathrm{Phase}}| \propto \sqrt{N \cdot \left[1 - \left(\frac{\sin(\sigma_P)}{\sigma_P}\right)^2\right]}$$
$$|\mathrm{SpICa}_{\mathrm{Phase}}| \propto \sqrt{N \cdot \left[1 - \left(\frac{1 - \cos^2(\sigma_P)}{\sigma_P^2}\right)\right]}. \tag{A8}$$

Approximating $\cos(t)$ with $-1\frac{t^2}{2}$

$$|\mathrm{SpICa}_{\mathrm{Phase}}| \propto \sqrt{N \cdot \left[1 - \left(\frac{\sigma_P^2 - \sigma_P^4/4}{\sigma_P^2}\right)\right]}$$
$$|\mathrm{SpICa}_{\mathrm{Phase}}| \propto \sqrt{N \cdot \left[\sigma_P^2/4\right]}$$
$$|\mathrm{SpICa}_{\mathrm{Phase}}| \propto \sqrt{N} \cdot \sigma_P. \tag{A9}$$

Similar to (A6), (A9) shows that for a constant SpICa performance, the required error will be inversely proportional to $\sqrt{N}$.

ACKNOWLEDGMENT

The authors acknowledge the contributions of NI for customized AWG. Access to CAD tools and technology was facilitated by MOSIS and CMC Microsystems. They are grateful to Prof. Vishal Saxena and Prof. Akbar Sayeed for useful comments.

REFERENCES

[1] P. Yang, Y. Xiao, M. Xiao, and S. Li, "6G wireless communications: Vision and potential techniques," *IEEE Netw.*, vol. 33, no. 4, pp. 70–75, Jul. 2019.

[2] S. Parkvall, E. Dahlman, A. Furuskar, and M. Frenne, "NR: The new 5G radio access technology," *IEEE Commun. Standards Mag.*, vol. 1, no. 4, pp. 24–30, Dec. 2017.

[3] L. Zhang and H. Krishnaswamy, "Arbitrary analog/RF spatial filtering for digital MIMO receiver arrays," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3392–3404, Dec. 2017.

[4] M.-Y. Huang and H. Wang, "A 27-to-41 GHz MIMO receiver with N-input-N-output using scalable cascadable autonomous array-based high-order spatial filters for instinctual full-FoV multi-blocker/signal management," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 346–348.

[5] M.-Y. Huang, T. Chi, F. Wang, T.-W. Li, and H. Wang, "A full-FoV autonomous hybrid beamformer array with unknown blockers rejection and signals tracking for low-latency 5G mm-wave links," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2964–2974, Jul. 2019.

[6] S. Jain, Y. Wang, and A. Natarajan, "A 10 GHz CMOS RX frontend with spatial cancellation of co-channel interferers for MIMO/digital beamforming arrays," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 99–102.

[7] A. Ghaffari, E. E. A. M. Klumperink, F. van Vliet, and B. Nauta, "Simultaneous spatial and frequency-domain filtering at the antenna inputs achieving up to +10 dBm out-of-band/beam P1dB," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 84–86.

[8] N. Oshima, M. Kitsunezuka, K. Tsukamoto, and K. Kunihiro, "A 30-MHz–3-GHz CMOS array receiver with frequency and spatial interference filtering for adaptive multi-antenna systems," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 362–373, Feb. 2017.

[9] M. Sayginer and G. M. Rebeiz, "An eight-element 2–16-GHz programmable phased array receiver with one, two, or four simultaneous beams in SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4585–4597, Dec. 2016.

[10] K. Kibaroglu, M. Sayginer, T. Phelps, and G. M. Rebeiz, "A 64-element 28-GHz phased-array transceiver with 52-dBm EIRP and 8–12-Gb/s 5G link at 300 meters without any calibration," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5796–5811, Dec. 2018.

[11] J. H. C. van den Heuvel, J.-P.-M. G. Linnartz, P. G. M. Baltus, and D. Cabric, "Full MIMO spatial filtering approach for dynamic range reduction in wideband cognitive radios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 11, pp. 2761–2773, Nov. 2012.

[12] S. Krone and G. Fettweis, "Energy-efficient A/D conversion in wideband communications receivers," in *Proc. IEEE Veh. Technol. Conf. (VTC Fall)*, Sep. 2011, pp. 1–5.

[13] M.-K. Cho, I. Song, and J. D. Cressler, "A true time delay-based SiGe bidirectional T/R chipset for large-scale wideband timed array antennas," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 272–275.

[14] S. Jang, R. Lu, J. Jeong, and M. P. Flynn, "A 1-GHz 16-element four-beam true-time-delay digital beamformer," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1304–1314, May 2019.

[15] Aurangozeb, F. Aryanfar, and M. Hossain, "A quad-channel 11-bit 1-GS/s 40-mW collaborative ADC enabling digital beamforming for 5G wireless," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3798–3820, Sep. 2019.

[16] D. C. M. Horvat, J. S. Bird, and M. M. Goulding, "True time-delay bandpass beamforming," *IEEE J. Ocean. Eng.*, vol. 17, no. 2, pp. 185–192, Apr. 1992.

[17] E. Ghaderi, A. S. Ramani, A. A. Rahimi, D. Heo, S. Shekhar, and S. Gupta, "An integrated discrete-time delay-compensating technique for large-array beamformers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3296–3306, Sep. 2019.

[18] W. K. Pratt, J. Kane, and H. C. Andrews, "Hadamard transform image coding," *Proc. IEEE*, vol. 57, no. 1, pp. 58–68, Jan. 1969.

[19] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in spatio-spectral-filtering MIMO receiver arrays for digital beamforming," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3152–3166, Dec. 2016.

[20] A. El Sayed *et al.*, "A Hilbert transform equalizer enabling 80 MHz RF self-interference cancellation for full-duplex receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 1153–1165, Mar. 2019.

[21] M. Mansuri *et al.*, "A scalable 0.128–1 Tb/s, 0.8–2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3229–3242, Dec. 2013.

[22] M. Mansuri *et al.*, "Strong injection locking of low-Q LC oscillators," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 699–702.

[23] A. Sharkia, S. Mirabbasi, and S. Shekhar, "A Type-I Sub-Sampling PLL With a 100 × 100 μm^2 footprint and -255-dB FOM," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3553–3564, Dec. 2018.

[24] O. Bakr and M. Johnson, "Impact of phase and amplitude errors on array performance," EECS Dept., Univ. California, Berkeley, CA, USA, Tech. Rep. UCB/EECS-2009-1, 2000.

Erfan Ghaderi (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2012, and the M.Sc. degree in circuits and systems from the University of Tehran, Tehran, in 2015. He is currently pursuing the Ph.D. degree in microelectronics at Washington State University, Pullman, WA, USA.

His current research interests include integrated circuit design for phased-array applications, time-domain signal processing, and high-speed data converters.

Ajith Sivadhasan Ramani (Member, IEEE) received the B.Tech. degree in electronics and communication engineering from the National Institute of Technology Karnataka, Mangalore, India, in 2014, and the M.A.Sc. degree in electrical and computer engineering from The University of British Columbia, Vancouver, BC, Canada, in 2017.

From 2014 to 2015, he worked with the Samsung Research Institute, Bengaluru, India. In 2018, he was at MaxLinear Inc., Vancouver. He is currently with the Semtech Signal Integrity Products Group, Burlington, ON, Canada, where he works on high-performance mixed-signal integrated circuits for high-speed I/O applications.

Arya A. Rahimi (Student Member, IEEE) received the B.S. and M.S. degrees from Washington State University, Pullman, WA, USA, in 2013 and 2019, respectively, where he is currently pursuing the Ph.D. degree at the School of Electrical Engineering and Computer Science.

His research is focused on wireless body sensor networks (WBSNs), biosignal acquisition, ultralow-power analog signal processing, and adaptive sampling architectures using classification algorithms.

Deukhyoun Heo (Senior Member, IEEE) received the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2000.

In 2000, he joined National Semiconductor Corporation, Santa Clara, CA, USA, where he was a Senior Design Engineer involved in the development of silicon ICs for cellular applications. Since Fall 2003, he has been a Professor with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA. He has around 180 publications, including 70 peer-reviewed journal articles and 110 international conference papers. He has primarily been interested in wireless and wireline data communications, battery-less wireless sensors, intelligent power management systems, and adaptive beamformers for phased-array communications.

Dr. Heo has been a member of the Technical Program Committee of DATE, International Microwave Symposium (IMS), and International Symposium on Circuits and Systems (ISCAS). He was a recipient of the National Science Foundation (NSF) CAREER Award in 2009. He has been appointed as the Frank Brands Analog Distinguished Professor since January 2017. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He is serving as an Associate Editor for the IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

Sudip Shekhar (Senior Member, IEEE) received the B.Tech. degree from IIT Kharagpur, Kharagpur, India, and the Ph.D. degree from the University of Washington, Seattle, WA, USA, in 2003 and 2008, respectively.

From 2008 to 2013, he was with the Circuits Research Laboratory, Intel Corporation, Hillsboro, OR, USA, where he worked on high-speed I/O architectures. He is currently an Associate Professor of electrical and computer engineering with the The University of British Columbia, Vancouver, BC, Canada. His current research interests include circuits for high-speed electrical and optical I/O interfaces, frequency synthesizers, and wireless transceivers.

Dr. Shekhar was a recipient of the IEEE Solid-State Circuits Society (SSCS) Predoctoral Fellowship from 2007 to 2008, the Intel Foundation Ph.D. Fellowship from 2006 to 2008, the Analog Devices Outstanding Student Designer Award in 2007, the Young Alumni Achiever Award by IIT Kharagpur in 2019, and the IEEE Transactions on Circuit and Systems Darlington Best Paper Award in 2010. He was a co-recipient of the IEEE Radio frequency IC Symposium Best Student Paper Award in 2015. He serves on the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC), the Custom Integrated Circuits Conference (CICC), and the Optical Interconnects (OI) Conference.

Subhanshu Gupta (Senior Member, IEEE) received the B.E. degree from the National Institute of Technology (NIT), Trichy, India, in 2002, and the M.S. and the Ph.D. degrees from the University of Washington, Seattle, WA, USA, in 2006 and 2010, respectively.

From 2011 to 2014, he was with the Radio Frequency Integrated Circuits Symposium (RFIC) Group, MaxLinear Inc., Vancouver, BC, Canada, where he worked on silicon transceivers and data converters for cable/satellite communication radios. He is currently an Assistant Professor of electrical engineering and computer science with Washington State University, Pullman, WA, USA. His research interests include wideband transceivers, energy-efficient circuits and systems, and stochastic hardware optimization techniques.

Dr. Gupta was a recipient of the National Science Foundation CAREER Award in 2020. He received the Analog Devices Outstanding Student Designer Award in 2008 and the IEEE RFIC Symposium Best Student Paper Award (Third Place) in 2011. He has served as a Guest Editor for the IEEE TRANSACTIONS OF CIRCUITS AND SYSTEMS—I and the *IEEE Design and Test Magazine* in 2019. He is serving as an Associate Editor for the IEEE TRANSACTIONS OF CIRCUITS AND SYSTEMS—I for the term of 2020–2021.