From Battery Enabled to Natural Harvesting: Enzymatic BioFuel Cell Assisted Integrated Analog Front-End in 130nm CMOS for Long-Term Monitoring

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Abstract—Biofuel cell as a natural energy source is a promising biocompatible technology which harvests the blood glucose into usable energy and replaces the toxic lithium-based battery solutions. However, the promise of this perennial non-toxic power is tempered by its unstable operation and low-voltage outputs leading to very limited operational lifetimes. This paper demonstrates a glucose-powered analog front-end with superior noise performance, which is enabled by standalone enzymatic biofuel cells operating for more than 30 min on active power without replenishment. Two biofuel cells are stacked to realize 0.5V output using commercially available glucose oxidase and the enzyme stability is improved via multipoint crosslinks by glutaraldehyde. To mitigate the effects of noisy and temperature-sensitive pseudo-resistors, a switched-resistor biasing scheme is applied to the input amplifier with the measured input-referred noise of 0.31 μV_{RMS} only. The proposed hybrid power scheme uses 1.6 μW from the battery with 1.9 μW provided by the biofuel cells. The entire analog front-end including a cascaded dual-supply amplifier with switched-capacitor SAR ADC and single-opamp relaxation oscillator occupies 1.12 mm^2. Measured results show on-chip gain and noise variations across temperature of only 1.1 dB and 19.2 nV/$\sqrt{\mathrm{Hz}}$, respectively, with noise (power) efficient factor of 1.46 (1.63).

Index Terms—Natural energy harvesting, glucose bio-fuel cell, low-noise, low-power instrumentation amplifier, switched-resistor, split-DAC ADC, single-opamp relaxation oscillator.

I. INTRODUCTION

THE emergence of ultra-low power analog processing techniques for bioelectronics in the past decade has deepened interests in sustainable power sources and energy scavenging systems for long-term monitoring and persistent sensing [1]–[7]. Biofuel cell for ultra-low-power CMOS

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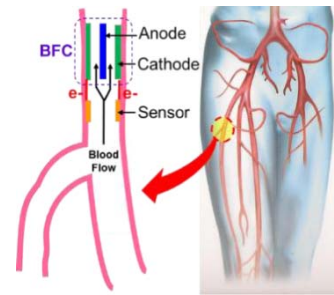Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Fig. 1. Future perennially powered BFC-systems 'producing' usable energy on-demand from body glucose.

devices is a promising biocompatible technology which harvests the blood glucose into usable energy and can replace the toxic lithium-based battery solutions. Compared to traditional batteries supplying each sensor node, the design of a biofuel cell (BFC) uses biocompatible enzyme-based electrodes (instead of expensive noble metal-based electrodes or toxic lithium ions) and can be a significant contributor towards future green nodes. Fig. 1 shows an approach towards future perennially powered enzymatic BFC-systems 'producing' usable energy on-demand from the body glucose and, ultimately, enabling unlimited functional lifetimes. Previous works have demonstrated the highest BFC potentials of around 0.2V-0.3V [8]–[11] with current outputs of a milli-Ampere. However, they exhibit poor long-term stability when loads are applied because the enzymes can be easily denatured and lose their catalytic functionality under various chemical and physical stresses imposed by the practical cell operating conditions. In this study, we present a contrasting approach with custom-designed stacked potential boosted BFC cells capable of micro-Ampere current output with an improved enzyme stability by introducing multipoint crosslinks.

We propose a low-noise sensitive microwatt front-end with superior noise- and energy-efficiencies using BFC to supplement the battery source while demonstrating operation for more than 30 minutes without any glucose replenishment. Section II describes briefly BFC construction methodology and design principles for long-term stability with manufacturing
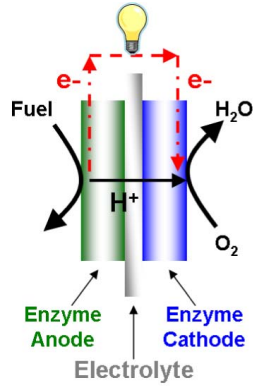
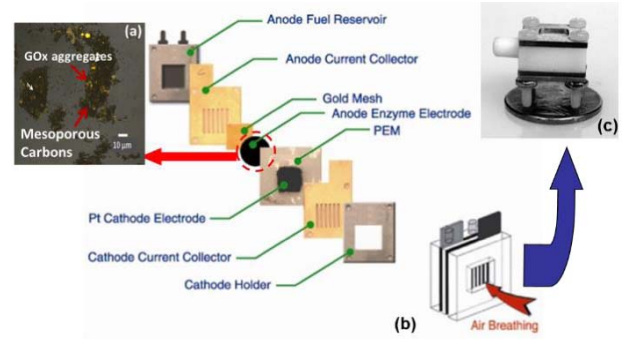Fig. 2.   Operating principle of enzymatic biofuel cells.

Fig. 3.   (a) The confocal image of the Glucose Oxidase (GOx)-nanocomposites, (b) the biofuel cell assembly with the anode enzyme electrode, and (c) the assembled single biofuel cell is smaller than a quarter-sized coin. The GOx is originated from *Aspergillus niger* and purchased from Sigma Aldrich: Cat#G7141 [17].

steps. Section III describes the desired system specifications for a BFC enabled analog front-end (AFE) with a focus towards long-term monitoring. The limitation with low-current and low-voltage outputs from the BFC is overcome using a stacked voltage cell to realize an energy-efficient design of the AFE. Section IV illustrates the design techniques for the AFE with an on-chip relaxation oscillator and an analog-to-digital converter. Measurement results of the sensor front-end with BFC are presented in Section V, followed by conclusion and scope for future works in this exciting area in Section VI.

II. DEVELOPMENT OF ENZYME ELECTRODE-BASED BIOFUEL CELL AND ITS PERFORMANCE

Fig. 2 illustrates the working principle behind an enzymatic biofuel cell. It consists of three main components: an enzyme anode, an electrolyte, and an enzyme cathode. There are three principal enzyme electrode requirements for achieving high power density: 1) a high density of enzyme bound to the electrode surface, 2) a high electron transfer rate between the active site of the enzyme and the conductive electrode surface, and 3) a high mass transfer rate of reactants and products to and from the bound enzyme active sites [12]. While achieving all these requirements, the enzyme activity must be stabilized for the long-term operation to be achieved. To meet some of these requirements, various techniques have been developed by previous investigators to create functional BFC electrodes such as immobilizing the enzyme on the external surface of nanotubes, entrapping it in sol-gel or polymers, or chemically modifying structures of enzymes [13]–[15]. The typical BFCs suffer from their low reliability because the enzymes used to construct their electrodes can easily denature (i.e., die) by losing their unique tertiary structure under various external stresses (e.g., temperature, shear, pH, concentration, and pressure stresses). Unlike these conventional BFC designs, our current work in this manuscript fabricates the enzyme electrode using the unique Glucose Oxidase (GOx)-nanocomposite technique. This technique enhances the long-term stability of enzymes within the BFC electrode by forming the protein nanoparticles and encapsulating them within the mesoporous carbon network.

We used enzyme precipitation coating method to form GOx enzyme aggregates [11]. These GOx aggregates were entrapped by Graphitized Mesoporous Carbon (GMC) to form the GOx-nanocomposites as shown in Fig. 3(a) [16]. Our previous work suggests that nanocomposite structure offered both improved electrochemical performance and stability by combining the high electrical conductivity offered by the GMC network with the high enzyme loading and stability offered by the cross-linked GOx aggregates. Finally, the GOx-nanocomposites were used to prepare the anode enzyme electrode for the biofuel cell as shown in Fig. 3(b) [17]. Fig. 3(c) shows the assembled quarter-sized BFC. For this study, we only utilized the enzyme electrode design for the anode side of BFC to demonstrate our electrode design concept. However, we can apply a similar enzyme electrode design used for GOx for fabricating the cathode enzyme electrode using oxygen reducing enzymes (e.g., laccase). By integrating both anode and cathode enzyme electrode into well-established microfabrication technologies, one can design the complete BFC that could be implanted into the human blood vessel as shown in Fig. 1.

The total output power of BFC is dependent on the surface area of electrodes assuming there is no mass transfer limitation. As the surface area of the electrode increases, the number of the active site (i.e., the number of enzymes) increases. Assuming there are no mass transfer limitations of glucose fuels at the anode and oxygen from the air at the cathode, then these increased number of active sites should lead to increased power output as more glucose fuels can be oxidized for releasing increased numbers of electrons. In our design, the geometric surface area of the anode and cathode are about 0.332 cm^2.

III. DESIGN CONSIDERATIONS FOR ELECTRONIC SENSOR

This section describes the design considerations for interfacing the analog front-end (AFE) to the BFC. The focus of this work is to present efficiency enhancements using a low-voltage dual-supply low-noise instrumentation amplifier (LNIA) without any charge-pump action while achieving significant battery energy savings.

Simultaneously, it explores interoperability of the enzymatic biofuel cell with the CMOS electronics as illustrated in the
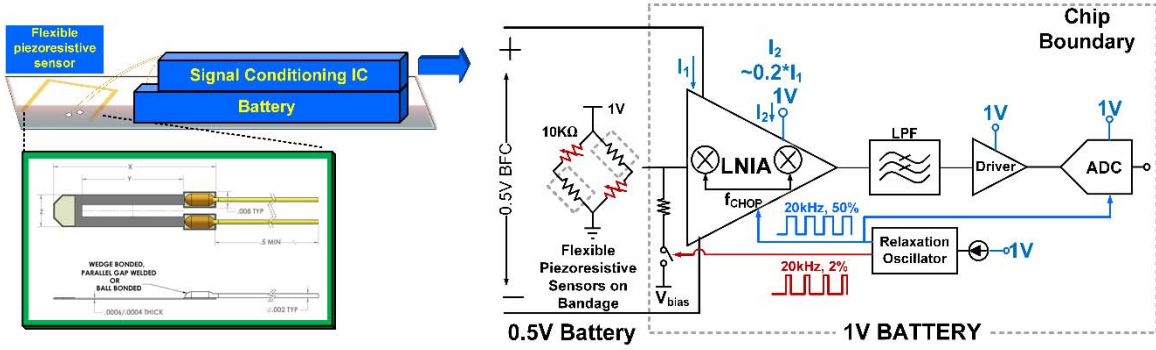
Fig. 4. Proposed schematic of crystal-free integrated sensor enabled by the 0.5V enzymatic stacked-biofuel cell and a 1V external battery. Interfacing the stacked biofuel cell with the readout sensor achieves greater than 60% power savings from the external battery source. The designed system is interfaced with a highly sensitive semiconductor strain gauge (gage factor $= 175 + / - 10$) attached to a flexible Tegaderm bandage.

next section. Fig. 4 shows the system diagram of the proposed sensor front-end powered by the BFC measuring strain using a semiconductor piezo-resistive sensor (PZR). The AFE comprises a dual-supply chopper-stabilized two-stage LNIA coupled to an on-chip temperature compensated relaxation oscillator (ROSC), a passive low-pass filter (LPF), and an intermediate driver stage followed by a low-input capacitance successive-approximation register analog-to-digital converter (ADC). The chopper stages in the LNIA and the ADC are clocked by the ROSC with an additional clock input (from the ROSC) feeding the biasing network for the LNIA. The BFC (0.5V) supplies the power-hungry stage in the LNIA and the rest is supplied by the battery (1V). Although the entire circuit can be energized only by the BFC, we chose to power the 1V supply with battery mainly because of the following reasons: 1) good power supply rejection ratio (PSRR) of the LNIA still needs to be maintained using a higher energy supply as there are no on-chip voltage regulators; 2) higher energy supplies can certainly be realized by stacking more number of BFCs, however, due to the current mismatch between individual cells, the output power efficiency might be degraded and thus reduce the operational times, and 3) combination of BFC and the battery creates two power domains such that the crosstalk between the oscillator, the ADC (typically noisy) and the LNIA can be reduced. Further research is still ongoing to completely eliminate battery without significant performance degradation.

Two off-chip highly sensitive PZR each of 10kΩ resistance and two on-chip poly resistors of equal resistance are connected in a Wheatstone Bridge configuration interfaced with the LNIA and attached to a flexible Tegaderm bandage to measure impedance changes due to strain as described in Section V. Semiconductor strain gages [18] are demonstrated to be more suitable for low noise strain sensing applications with a RMS noise floor of $0.04\mu\varepsilon$ within a 1kHz bandwidth, which is $50\times$ lower than foil strain gages. This corresponds to an integrated voltage noise of $3.5\mu V_{RMS}$ within the 300Hz bandwidth. The noise from readout circuits thus cannot be neglected unless it contributes no more than 0.35μVRMS (based on the rule of thumb of 10 to 1 ratio). The voltage and strain relationship within the Wheatstone bridge configuration
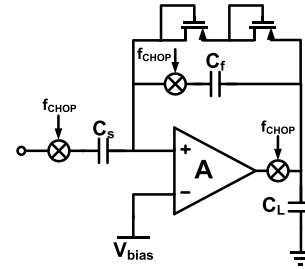

Fig. 5. Conventional capacitively-coupled low-noise instrumentation amplifiers (LNIA) with chopper stabilization.

is shown as below:

$$V = \varepsilon * GF * \frac{V_b}{2}$$

where ε is the strain applied, GF is the gage factor of the strain gage, and V_b is the voltage supply of Wheatstone bridge. The full-scale output of the strain gage is calculated to be 1mV thereby required 45dB dynamic range (DR) with an 8-bit ADC.

IV. PROPOSED DUAL-SUPPLY LOW-NOISE ENERGY-EFFICIENT ANALOG FRONT-END

This section describes the design of the individual components of the AFE including LNIA, ROSC, and the ADC. Using low-voltage supply provided by the BFC, we first analyze the use of switched-resistors and its sensitivity to noise and temperature variation in comparison to pseudo-resistors.

A. Effects of Leakage and Temperature Sensitivity on Pseudo-Resistors in Comparison to Switched-Resistors

Past decade has seen wide usage of pseudo-resistor based capacitively-coupled LNIA in biophysiological signal monitoring applications [19]–[28]. As shown in Fig. 5, it comprises of an opamp (A) in a capacitive feedback network biased by GΩ pseudo resistors in subthreshold region with chopper stabilization stages [29]. Chopper stabilization is widely used to reduce the $1/f$ noise of the opamp and the DC offset to a first-order. An important consideration at low-supply
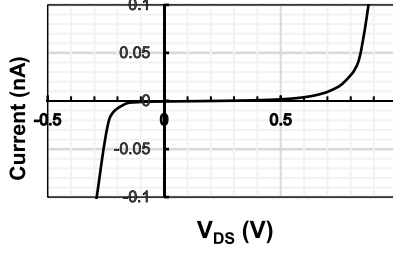
Fig. 6.   Simulated current-voltage relationship of a pseudo-resistor at room temperature.

Fig. 7.   Simulated results of resistance variation of a pseudo-resistor with respect to temperature.

voltages is the second-order effect of the PVT-dependent bulk leakage in the pseudo-resistor that creates nonlinearity due to temperature sensitivity leading to significant resistance variation across temperature.

Pseudo resistors shown in Fig. 5, though an area efficient way to implement on-chip GΩ resistance based on their ultra-low subthreshold leakage currents suffer from the voltage swing dependent subthreshold leakage which tends to be highly nonlinear. This limits the DR and noise sensitivity of the overall system. In addition, its subthreshold based leakage could vary by approximately $100\times$ across temperature. The resistance of the pseudo resistors can be derived from the MOSFET subthreshold current equation,

$$I_D = K \cdot V_T^2 \cdot \exp\left(\frac{V_{GS}}{nV_T}\right) \cdot \left[1 - exp\left(\frac{-V_{DS}}{nV_T}\right)\right] \quad (1)$$

where K is a device related parameter, V_T is the thermal voltage which equals to kT/q, n>1 is a nonideality factor. Differentiation by V_{DS} yields g_{ds}:

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = K \cdot V_T \cdot \left[\frac{1}{n} \cdot exp\left(\frac{V_{DS}}{nV_T}\right) - \frac{(1-n)}{n} \cdot V_T \right.$$
$$\left. \cdot exp\left(\frac{(1-n) \cdot V_{DS}}{nV_T}\right)\right] \quad (2)$$

which is exponentially proportional to V_{DS} from (2). Fig. 6 shows the simulated subthreshold leakage variation of a pseudo-resistor at room temperature against change in V_{DS}.

Temperature dependency can also be derived by differentiating g_{ds} by temperature, written as below.

$$\frac{\partial g_{ds}}{\partial T} = K \cdot \frac{1}{n} \cdot \left[\left(\frac{k}{q} - \frac{V_{DS}}{nV_T}\right) \cdot exp\left(\frac{1}{n} \cdot \frac{qV_{DS}}{kT}\right) - (1-n)\right.$$
$$\left. \cdot\left(\frac{k}{q} - \frac{1-n}{n} \cdot \frac{V_{DS}}{T}\right) \cdot exp\left(\frac{1-n}{n} \cdot \frac{qV_{DS}}{kT}\right)\right]$$

The above equation only considers the first-order temperature dependency of thermal voltage and ignores the second-order effects such as carrier mobility. Fig. 7 shows the simulated results of the temperature coefficient of pseudo-resistors with a constant V_{DS} of 100mV. A $215\times$ incremental effective resistance from 100°C to 0°C yields a temperature coefficient of $2.15\times$/ °C.

This PVT dependency of pseudo-resistors has limited the LNIA performance in high DR applications and systems operating under a wide range of temperatures. In this work,
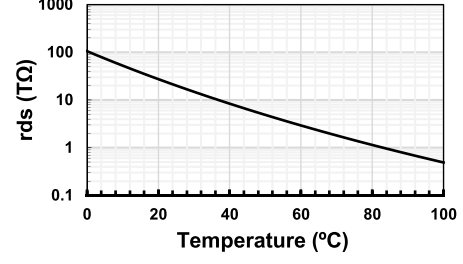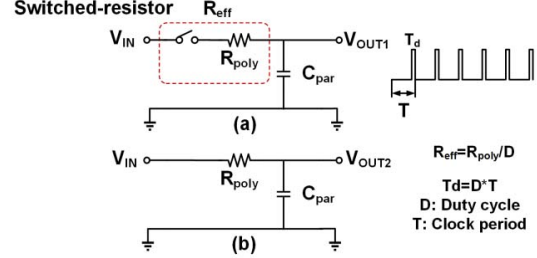

Fig. 8.   Switched-resistor with a periodic pulse switching system.

we replace the PVT-sensitive pseudo-resistors with switched-resistors implemented by a duty-cycled switch and a poly-resistor (R_{poly}) in series based on a periodic pulse switching system [30] shown in Fig. 8. The clock is directly coupled to on-chip low temperature-coefficient ROSC with an output pulse width duty-cycled at 2% [31]. The 2% duty-cycle is selected to avoid any dividers in the ROSC clock output and add more mismatch at higher power consumption. The LNIA is directly coupled to the buffered internal node of the ROSC as discussed further in Section IV.C. As the switch is driven by a pulsed clock with a duty cycle of D, the effective resistance R_{eff} is boosted by $1/D$ given by $R_{eff} = R_{poly}/D$. A large resistance can be implemented, especially in low frequency applications. The small duty cycle required can be easily realized with minimal circuit overhead as described in Section IV.

Obviating the need for any pseudo-resistors, this design leads to a temperature-stable implementation with low leakage. With a 2% duty-cycle clock, the R_{poly} that is used to implement the switched-resistor is about 1MΩ. The switched-resistor consumes an area of 20×20 μm^2 and is implemented with poly-resistors.

Interested readers can refer the seminal work by Kaehler [30] for the analysis of switched-resistors in both time and frequency domain and its impact to the LNIA noise. Chandrakumar [25] recently used Fourier transform to analyze the switched resistor circuits yielding an effective resistance:

$$R_{eff_{switched}} = T/T_d \cdot R_{poly} = D \cdot R_{poly}$$

This change reduces the required passive resistance, R_{poly}, by the duty-cycle factor. In our design, as the ROSC outputs a 2% duty-cycle clock, the effective resistance is observed to be amplified by $50\times$. In standard CMOS process, the temperature

coefficient of a poly-resistor can be as low as 500ppm/°C while the pulse variation due to temperature in the ROSC is 20ppm/°C, resulting in an overall temperature coefficient as low as 1%/°C which is approximately $200\times$ better than the pseudo-resistors. Further improvements can be made using poly-resistors with positive- and negative-temperature coefficients. It is also significant to analyze the switched-resistors noise contribution as it is used in low-noise applications for most of the cases. The switched-resistor operates as a sample-and-hold circuit similar to switched-capacitor circuits. The noise contributed by the effective resistance R_{eff} being sampled on the capacitor has a power spectral density of $4kT R_{eff}$ with a bandwidth determined by R_{eff} and C_{par}. Therefore, the total noise contributed by switched-resistors, kT/C_{par}, is the same as in sample-and-hold. Thus, in order to minimize the noise floor of a switched-resistor, a large sampling capacitor is still required.

B. Proposed Two-Stage Dual-Supply BFC-Enabled LNIA

1) Semi-Pseudo-Differential 1st Stage Preamp: Recent state-of-the-art LNIAs have employed two-stage dual-supply amplifiers for demonstrating higher noise- and power efficiencies. The low-noise current-hungry first stage preamplifier operated at low supply voltages followed by a high-noise low-power second stage amplifier operating with a high supply voltage breaks the trade-off between power-efficiency and noise-efficiency. Yaul and Chandrakasan [26] recently demonstrated a two-stage LNIA with a 0.2V pseudo-differential first stage biased using pseudo-resistors and a high-gain second-stage amplifier. The two-stage dual supply topology realized low-noise with good power efficiency and common-mode rejection ratio (CMRR) using beyond-rail biasing. However, a low-pass corner formed by pseudo-resistor in the common-mode feedback loop leads to a frequency dependent pole that results in poor settling. For applications using aggressive duty-cycling, this turn-ON time adversely limits the overall performance. The pseudo-differential design further limits the PSRR thus on-chip switching regulators are implemented at the cost of power and area overhead. Chandrakumar and Marković [25] replaced pseudo-resistors by switched-resistors. However, without any on-chip clock generator, the generation of nanosecond pulses is susceptible to process variations requiring manual calibration steps.

In this work, a two-stage dual-supply chopper-stabilized LNIA topology is used. The first-stage current-intensive preamplifier is powered up by the BFC with the second stage amplifier still enabled by the battery. This arrangement enables more than 60% savings in power and saves precious battery resources limited currently by the BFC. While future implementations of BFC will enable replacing the battery completely, this work illustrates superior noise- and power-efficiencies using this dual-supply feature.

Fig. 9(a) shows the proposed LNIA followed by a passive RC LPF and a driver stage. The entire cascaded two-stage amplifier is capacitively coupled with an embedded chopper stabilization stages. The chopping frequency is selected to be 20kHz (twice the flicker noise corner frequency) generated
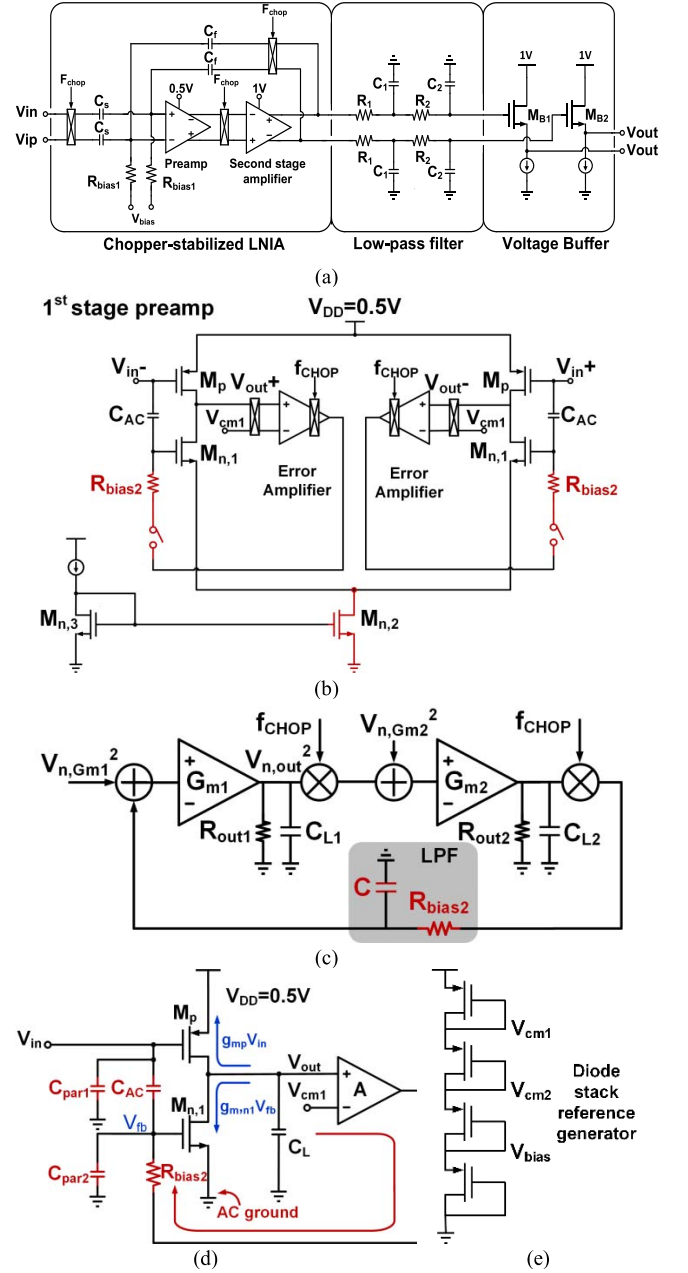

Fig. 9. (a) Proposed two-stage chopper-stabilized low-power, low-noise LNIA with passive filter and a buffer for off-chip drive, (b) detailed circuit diagram of the 1st stage preamp with switched-resistor biasing, (c) signal flow diagram of the proposed pre-amplifier, (d) single-ended representation of the proposed LNIA, and (e) on-chip reference generator using stacked PMOS diodes.

from the on-chip nanowatt ROSC which will be discussed later. V_{bias} is generated on-chip to bias the PMOS devices inside the first-stage preamplifier through a large resistor R_{bias1}. C_s together with R_{bias1} forms a high-pass filter whose corner frequency is set one order of magnitude smaller than the chopped input signal frequency (20kHz) to avoid any attenuation to the input signal. R_{bias1} and C_s are chosen to be 50MΩ and 10pF respectively, forming a high pass frequency at around 300Hz. Therefore, C_f is set to be 100fF to achieve a closed loop gain of 40dB.

We illustrate a semi-pseudo differential inverter-based preamplifier enabled by the 0.5V BFC without any supply boosting. The pseudo-differential design with the tail current source ensures enough headroom on each transistor as shown in Fig. 9(b) while drawing $4.26\mu A$ in the simulation. The current reuse scheme enabled by the input complementary differential pairs approximately doubles the effective transconductance of the amplifier which consequently halves the input-referred noise. The output common mode voltage is set by an error amplifier (EA) to V_{cm1} through a feedback loop by controlling the gate bias voltage of M_{n1} DC coupled by a large resistor R_{bias2} implemented with the switched-resistor described in Section IV.A. Each of the EAs are chopper stabilized in the common-mode signal path and hence, do not contribute any additional offsets or flicker noise to the pre-amplifier input while consuming only 20 nW power. A preamp tail current source (M_{n2}) with temperature-compensated gate bias is used to enhance CMRR across temperature while reducing the effect of supply spurs. The tail current source reduces the effect of supply spurs compared to [26]. C_{AC} decouples the gate DC bias of M_p and M_{n1} to add an extra degree of freedom in the design.

From the single-ended representation of the pre-amplifier shown in Fig. 9(d), the input voltage V_{in} is directly coupled to the gate of M_p while it is AC coupled to the gate of M_{n1} through C_{AC}. C_{AC} forms a capacitive divider with C_{par2}, the parasitic capacitor at the gate of M_{n1}. The small signal voltage at the gate of M_p can be written as:

$$V_{g,n1} = \frac{C_{AC}}{C_{AC} + C_{par2}} * V_{in}$$

From the above, C_{AC} has to be large enough compared to C_{par2} to avoid any input signal attenuation. Biased in weak inversion for maximum g_m efficiency at the same current density level, the size of the input devices (M_p, M_{n1}) are typically large which makes its parasitics not negligible. Thus, we choose C_{AC} to be 5pF. Observing the feedback loop, there are two critical nodes in the pre-amplifier which creates a pole at the inverter output, and at the gate of M_{n1} (Fig. 9(d)). The inverter stage burns a large amount of current to reduce the noise floor, pushing the pole at its output far outside the bandwidth to be a non-dominant pole. The pole at the gate of M_{n1}, due to the large effective resistance of the switched resistor R_{bias2} and the large AC coupling capacitor, C_{AC} (as discussed above to ensure no signal attenuation), becomes the dominant pole and is typically well separated from the non-dominant pole. The stability of the loop thus won't be a major concern even without compensation. However, the dominant pole at the gate of M_{n1} severely affects settling and slow down the system transient response, especially in low power applications where the circuits can be aggressively duty-cycled. Therefore, it is essential to analyze the loop's frequency response. The feedback voltage, V_{fb} can be obtained by breaking the loop at the gate of M_p as follows:

$$V_{fb} = (g_{m,Mp} * V_{in} + g_{m,Mn1} * V_{fb}) * (R_{out}//1/sC_L) * A * \beta$$
(3)

$$\beta = \frac{1/sC}{1/sC + R_{bias2}} = \frac{1}{1 + s R_{bias2} C}$$
(4)
$$C = (\frac{1}{sC_{par1}} + \frac{1}{sC_{AC}})//\frac{1}{sC_{par2}}$$
$$R_{out} = r_{o,Mp}//r_{o,Mn1}$$

where $g_{m,Mp}$ ($r_{o,Mp}$) and $g_{m,Mn1}$ ($r_{o,Mn1}$) are the transconductance and output resistance of M_p and M_{n1} respectively, C_L is the load capacitance at the inverter output, A is the DC gain of the EA and C_{par1} is the parasitic capacitance at the gate of M_p. From (3), the loop gain is derived as:

$$LG = \frac{V_{fb}}{V_{in}} = \frac{g_{m.Mp} * (R_{out}//\frac{1}{sC_L}) * A * \beta}{1 - g_{m,Mn1} * (R_{out}//\frac{1}{sC_L}) * A * \beta}$$
(5)

Substituting (4) into (5) we can get

$$LG = \frac{g_{m,Mp} R_{out} A}{s^2 R_{out} R_{bias2} C^2 + s(R_{bias2} + R_{out})C + 1 - g_{m,Mn1} R_{out} A}$$

From above, the feedback loop forms a two-pole low-pass characteristic. For fast settling, the combination of C_{AC} and R_{bias2}, C_{par1} and C_{par2} cannot be too large. C_{AC} is set to 5pF as discussed above, thus R_{bias2} needs to be well-controlled to maintain an acceptable loop bandwidth and hence settling time across corners and temperatures. The merit of switched-resistors plays an important role in implementing R_{bias2}. As discussed in Section IV.A, the resistance of pseudo-resistors can vary up to $200\times$ from $0°C$ to $100°C$, which directly changes the loop bandwidth by $200\times$ proportionally. This severely limits the duty cycle of the overall system in ultra-low power applications. Fig. 10 shows the simulated loop bandwidth with respect to different R_{bias2} values from $1M\Omega$ to $200M\Omega$ to mimic the $200\times$ incremental effect in the resistance of pseudo resistor from $100°C$ to $0°C$, observing a decrease in loop bandwidth over $200\times$. Substituting the pseudo-resistor with switched-resistor, the incremental effect can be minimized thus creating a PVT constant settling behavior. In our design, R_{bias2} is set to 50 $M\Omega$. Fig. 9(c) shows the signal flow diagram of the proposed pre-amplifier. Though the EA will feedback its own noise to input, R_{bias2} together with C forms a low pass filter in the feedback path which greatly limits the noise bandwidth of the EA. The EA has negligible in-band noise contribution and the only active component that contributes to noise is the inverter-based amplifier. The inverter-based input complementary pairs are biased in weak inversion region to maximize its transconductance efficiency while drawing large current to reduce the input-referred noise voltage. Operating at 0.5V, it can draw $2\times$ current while still maintaining the same power consumption. Flicker noise, mismatch and offset at the preamplifier input in the differential signal path is mitigated through the chopper-stabilization stage at the input capacitor (coupled to the PZR) and the preamp output. The decoupling capacitor (C_{AC}) used between M_{n1} and M_p allows an extra degree of freedom to bias the preamp inputs.

All the reference voltages are generated on-chip. As the accuracy and line sensitivity is not a major concern here as long as all the transistors can operate with enough headroom, the references are generated using stacked-PMOS diodes in
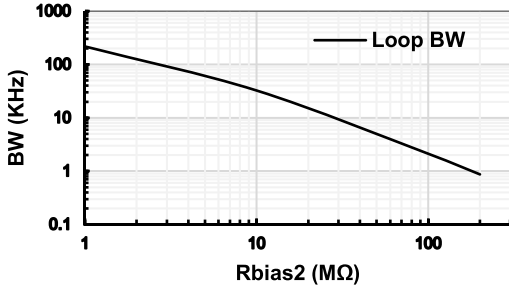
Fig. 10. Simulated variation of preamplifier loop bandwidth with 200× resistance variation of R_{bias2}.
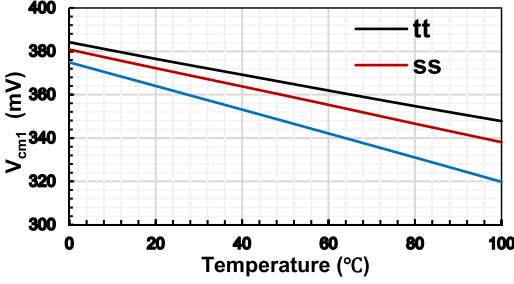

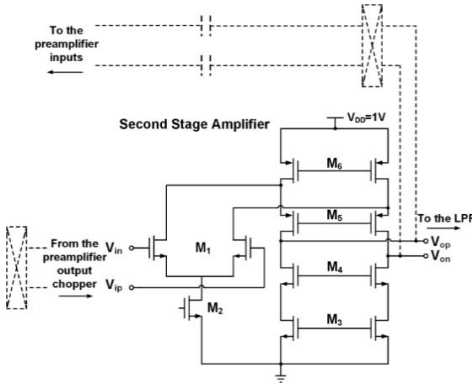Fig. 11. Simulated V_{cm1} variation across corners and temperatures.

Fig. 12. Second stage folded-cascode amplifier (biasing and common mode feedback not shown for simplicity).

subthreshold (Fig. 9(e)) consuming only 153nW using the 1V battery supply. The three generated voltages are V_{cm1}, V_{cm2} and V_{bias} with magnitudes 0.4V, 0.5V, 0.25V respectively. Fig. 11 shows the DC voltage of V_{cm1} across corners and temperatures and it can be observed that the headroom for M_p is large enough to maintain it operating properly.

2) Second-Stage Folded-Cascode Amplifier Design: The second-stage amplifier is designed using conventional single-stage folded-cascode topology as shown in Fig. 12 operating at 1V supply. It should be noted that its input-referred noise is divided by the preamp gain and thus has a relaxed design specification. NMOS input differential pairs are chosen to achieve highest g$_m$ efficiency with the same amount of current. Deep-Nwell devices are used for the input transconductance stages of both the first stage preamplifier and the second stage amplifier to minimize the substrate noise coupling effects. The two-stage design is optimized to minimize offset while

maximizing the transconductance. The overall input referred noise of the LNIA is approximately,

$$\frac{\bar{v_n^2}}{\Delta f} = \left(\frac{C_s + C_f}{C_s}\right)^2 \cdot \left[\frac{4kT\gamma}{g_{m,Mn1} + g_{m,Mp}}\right.$$
$$+ \frac{4kT\gamma}{g_{m,M1}\left(g_{m,Mn1} + g_{m,Mp}\right)^2 \left(r_{o,Mn1}//r_{o,Mp}\right)^2}$$
$$\left. + \frac{4kT\gamma\left(g_{m,M3} + g_{m,M6}\right)}{g_{m,M1}^2\left(g_{m,Mn1} + g_{m,Mp}\right)^2 \left(r_{o,Mn1}//r_{o,Mp}\right)^2}\right]$$

where $g_{m,M1}$ is the transconductance of second stage input differential pair, $g_{m,M3}$ and $g_{m,M6}$ is the transconductance of the two current sources of the folded-cascode amplifier respectively.

C. On-Chip Nanowatt Relaxation Oscillator Using Single-Opamp Constant Charge Subtraction

Relaxation oscillators (ROSC) are increasingly being used as a clock reference due to their low-power operation and ease of on-chip integration in standard CMOS processes [31]. In this section, we expand our recent work [32] using a single-opamp switched-current amplifier with constant charge subtraction technique which is proposed in [33] as shown in Fig. 13. The principle of operation is explained as below.

Assuming an initial condition when C_1 is fully discharged, the comparator, $Comp_1$, outputs a low setting the output of the R-S latch as $\Phi_1 = 1$ and $\Phi_2 = 0$. During $\Phi_1 = 1$, C_1 is charged by a constant current source, and C_2 is charged through a constant voltage source to a fixed voltage with the op-amp shorted. The comparator switches its state after C_1 is charged exceeding the $Comp_1$ threshold, V_{th1}. The output phases are now $\Phi_1 = 0$ and $\Phi_2 = 1$. During $\Phi_2 = 1$, C_2 is connected in feedback across the op-amp resulting in charge subtraction between C_2 and C_1. A constant charge will always be subtracted on C_1 during every cycle when Φ_2 is enabled as shown in Fig. 13. By charge conservation,

$$C_1 V_{th1} - C_2 V_{ref} = C_1 V \tag{6}$$

where V_{th1} is the comparator threshold voltage, V_{ref} is the subtracted voltage and V_{C1} is the input voltage of the comparator. Thus,

$$V_{C1} = V_{th1} - \frac{C_2}{C_1} V_{ref} \tag{7}$$

Therefore, as a constant voltage V_{ref} is subtracted from V. The resulting oscillating frequency is shown in (8) assuming C_1 and C_2 are equal.

$$f_{osc} = \frac{I_{ref}}{C_1 V_{ref}} \tag{8}$$

The constant-charge technique does suffer from higher power consumption as the op-amp needs a large bandwidth to enable good settling during Φ_2. In [33], the problem is solved by having two separate op-amps operating during different phases. Instead, we used a switched current technique [32] that enables only one op-amp to operate in two phases and still meet the fast settling requirement during Φ_2. Fig. 13 shows
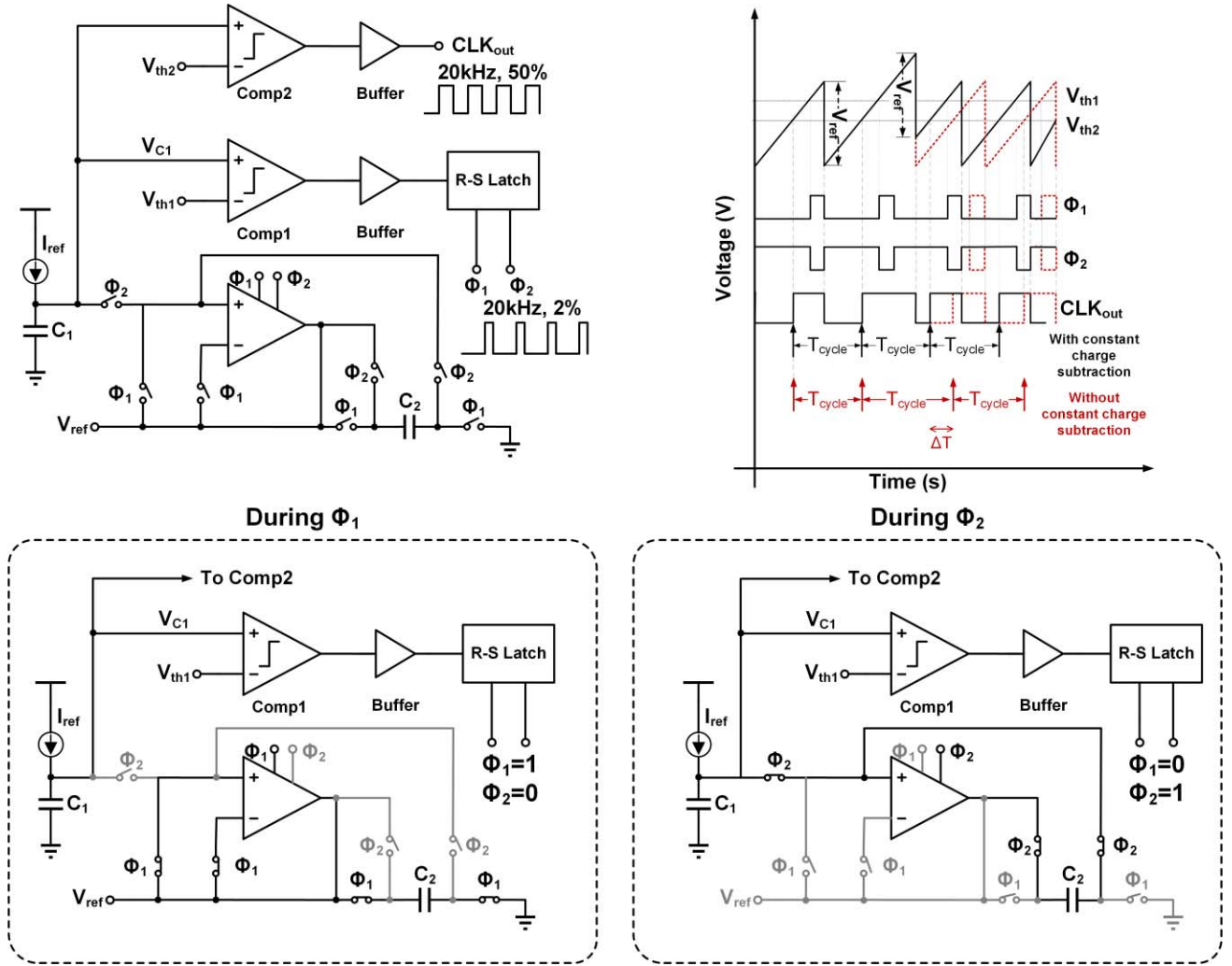
Fig. 13. Near-zero power relaxation oscillator using a single switched-current amplifier with 2%/50% duty-cycle clock output on the top [32] with its operation during different phases on the bottom, and the comparison of the timing diagram between the cases with constant charge subtraction scheme (black) and without constant charge subtraction (dashed red). A frequency variation of ΔT shows up in the later case due to the any delay variation of the comparator and buffer.

the circuit operation with the op-amp reference current supply being switched between two different current sources. The low power mode is enabled during Φ_1 to help preset the initial DC operating point and the high-power fast-settling mode is enabled during Φ_2 to accurately realize the charge subtraction. The settling time required in Φ_2 is shown in (9), where g_m is the effective trans-conductance of the op-amp and ε is the settling error.

$$t_s = \frac{C_1 // C_2 * \ln(\varepsilon)}{g_m} \tag{9}$$

A two-stage amplifier topology is chosen here due to a large input common mode range and output swing since the op-amp needs to tolerate a large swing at both the input and output (Fig. 13). Further discussion on flicker and thermal noise constraints can be obtained from [32]. Fig. 14 shows the simulated phase noise from the relaxation oscillator and it's temperature stability when operating at the 20kHz oscillation frequency. Both the 2%/50% duty-cycle clock outputs are generated by the described circuit without any additional
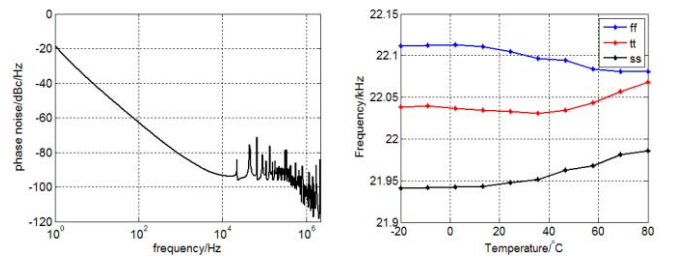
overhead and are used to activate the switched-resistor in the LNIA, the chopper switches, and the SAR-ADC.

D. Differential C-2C/Binary DAC Based SAR-ADC

An 8-bit differential successive approximation analog-to-digital converter (SAR-ADC) (Fig. 15) is implemented following the proposed LNIA and a second-order passive low-pass filter. The performance of the ultra-low-power subthreshold

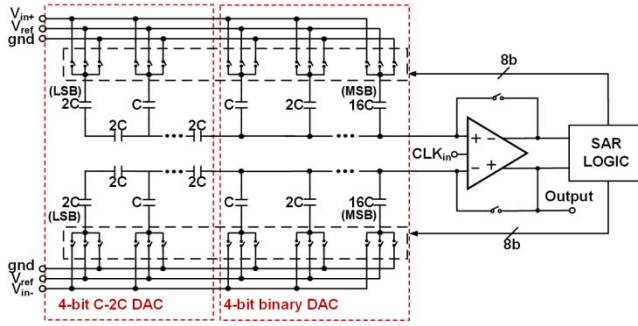Fig. 14. Simulated phase noise and ROSC temperature stability.

Fig. 15. Differential SAR ADC with an 8-bit split-DAC comprising of a 4-bit C-2C and a 4-bit binary DAC and an offset-canceled comparator.

ADC has been limited by the thermal noise and the input offset of the comparator. Conventional binary-DACs [34] with effective input capacitance ($= 2^n C_u$) occupies a large area and suffers from charge injection (C_u is the unit capacitor in the DAC). In contrast, the C-2C DAC structure [35] reduces the effective input capacitance to $2C_u$. The C-2C DAC architecture however suffers from poor matching and linearity. In our design, we chose a hybrid split-DAC structure with a 4-bit C-2C DAC (LSB) and a 4-bit binary DAC (MSB), resulting in lower input capacitance of $2^{n/2+1}C_u$. The unit capacitor is selected to be 77fF which yields an effective sampling capacitor of 2.5pF with an 8-bit DAC based on the thermal noise floor limitation, $\sqrt{\frac{kT}{C}} < \frac{1}{2} \cdot \frac{1}{2^n} \cdot V_{in}$, where V_{in} is the full-scale input signal.

The comparator preamplifier has an input-offset cancellation circuit to alleviate the flicker noise and the offset. By connecting the preamplifier in unity-gain feedback during the sampling phase, the offset voltage of the preamplifier is sampled and subtracted in the next phase, resulting in an effective offset voltage of V_{os}/A, where V_{os} is the preamplifier offset voltage and A is the preamplifier gain. The input differential devices are sized to be $60\mu m/1\mu m$ to further reduce the mismatch and flicker noise. The comparator as the only component that consumes static power has a power consumption of only 120nW. The buffer in between the LNIA and ADC provides isolation from clock feedthrough and kickback on the LNIA output.

V. MEASUREMENT RESULTS

The readout sensor IC is interfaced with a sensitive semiconductor PZR (gage factor $= 175 \pm 10$) manufactured by Micron Instruments. With the input chopper-stabilization, the LNIA input impedance at 5MΩ is sufficiently larger than the 10kΩ impedance of the PZR for this application avoiding loading effects. Fig. 16(a) shows the measured differential outputs of the readout sensor IC when interfacing with the BFC. A gain of around 100 is observed with an input of 1 mVpk-pk sine signal at the LNIA input meeting the design target of 40 dB. Fig. 16(b) further shows the response of the BFC when loaded. The BFC can provide a stable standalone output voltage for more than 30min. This can be further extended with continuous glucose replenishment. The readout sensor IC was fabricated in $0.13\mu m$ CMOS technology with an active area of
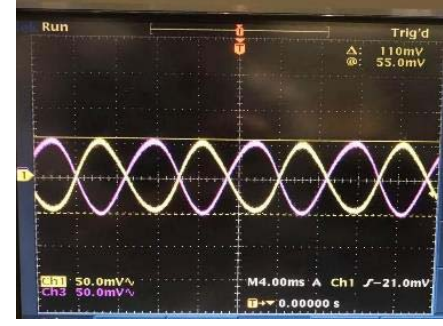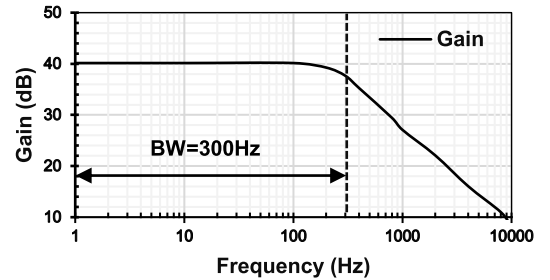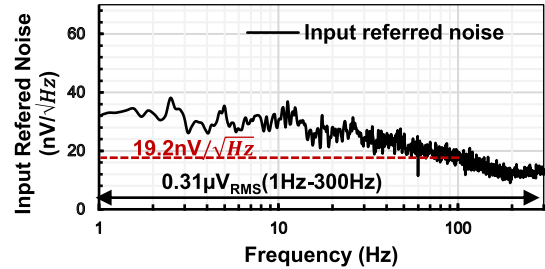

(a)
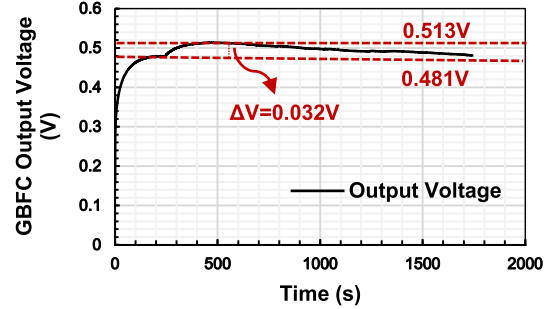
(b)

Fig. 16. (a) Measured LNIA output with an input of 1mV-pk-pk with an observed gain of 100, (b) GBFC output voltage under loading used in standalone condition. The denaturization is due to absence of glucose replenishment when it is operated in standalone condition.

(a)

(b)

Fig. 17. (a) Measured LNIA gain and CMRR, (b) Input-referred noise with $19.1nV/\sqrt{Hz}$ at 100 Hz with integrated noise from 1-300 Hz $0.31\mu V_{rms}$. DC offset in the measurement results in incran ease in close-in noise.

$1.12mm^2$ without pads. The active area without pads and decap is $0.8mm^2$ including LNIA, ADC, and ROSC. The dual-supply scheme with two power sources provides greater than 60% energy savings. The 0.5V BFC supply provides $1.9\mu W$ with the rest $1.61\mu W$ supplied by the 1V battery. Fig. 17(a) shows the measured LNIA gain frequency response at the output of

TABLE I
COMPARISON OF BFC ENABLED AFE+ADC WITH STATE-OF-THE-ART

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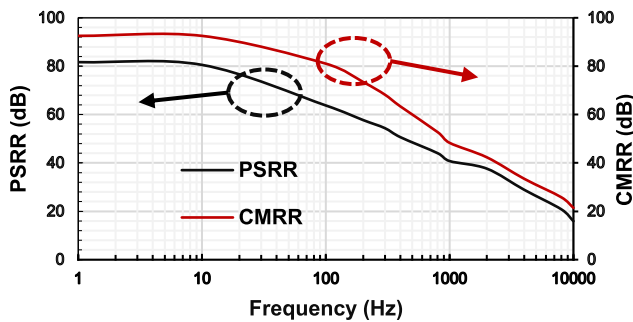|	[24]	[25]	[26]	[27]	[28]	**This work**
Process/ Publication	180 nm TBioCAS' 15	40 nm JSSC'17	180 nm ISSCC'16	65nm ISSCC'17	130 nm/500 nm TBioCAS' 12	**130 nm**
Supply (V)	0.3/0.6/1.2 (Batt)	1.2 (Batt)	0.2/0.8 (Batt)	1.2 (Batt)	1 (Batt)	**0.5 (BFC) / 1 (Batt)**
Area (mm²)	1.6 (LNIA/LDO/CP/Buff)	0.071 (LNIA only)	1 (LNIA/PGA/AAF)	16 (System)	0.047/0.046/0.072 (LNIA only)	**0.44 (AFE) 1.12 (Total)**
Gain (dB)	33	26	57.8	40	40.5/36.1/40	**40**
BW (Hz)	0.7-182	200/5000	670	250	0.4-8.5k/0.3-4.7k/0.05-10.5k	**300**
IRN (nV/$\sqrt{Hz}$)	24.4	80 @ 200 Hz	36 (0.5-670)	--	-	**19.2 @ 100 Hz**
Integr. IRN (uVrms)	0.34/1.01	2 (1-200 Hz) 7 (200-5000Hz)	0.9 4 (0-670 Hz)	0.44 (0.5-100)	3.2/3.6/2.2	**0.31 (1-300 Hz)**
IRN drift across temp (%/ºC)	-	-	0. 7 @ 100 Hz*	-	-	**0.4 @100Hz**
Gain drift across temp (%/ºC)	-	-	0.057 @ 100 Hz*	--	-	**0.039 @ 100 Hz**
CMRR (dB)	>70	-	85	>110	60/-/80	**92**
PSRR (dB)	>70	-	80		60>/5.5/>80	**82**
Power (µW)	1.17/0.3	2 (Batt)	0.79 (Batt)	5.4	12.5/0.8/12.1	**1.9 (GBFC) 1.61 (Batt)**
NEF/PEF[1]	1.74/1.05	4.9/7	2.1/1.6	3.59/--	4.5/1.9/2.9/-	**1.46/1.63**
Blocks	LNIA/LDO/ Charge pump/Buff	LNIA only	LNIA/PGA[2]/ AAF[3]	System-on-Chip	LNIA only	**LNIA/Buff/ ADC/ROSC**
[1]$NEF = V_{RMS}\sqrt{\frac{2*I_{total}}{\pi*4kT*V_T*BW}}$ $PEF = \frac{2*V_{RMS}^2}{\pi*4kT*V_T*BW}*P_{total}$ V_T–Thermal Voltage						
* Estimated [2]PGA – Programmable Gain Amplifier, [3]AAF-Anti-Aliasing Filter						

Fig. 18.   Measured LNIA PSRR and CMRR of >80dB.

Fig. 18. Measured LNIA PSRR and CMRR of >80dB.

Fig. 19.   Measured LNIA gain and input-referred noise with temperature variation from 25-100°C.

the off-chip buffer with a loading capacitor of 47nF in order to limit the bandwidth due to the high-current low-noise design of the first stage preamplifier. The measured gain profile shows a droop at 200Hz due to extra package parasitics. The response shows a single-pole response of 20dB/decade between 300Hz-10kHz.

An input-referred noise density of only $19.1 nV/\sqrt{Hz}$ is measured at 100Hz with the total integrated input-referred noise in the 1-300Hz bandwidth measured to be $0.31 \mu V_{rms}$ as
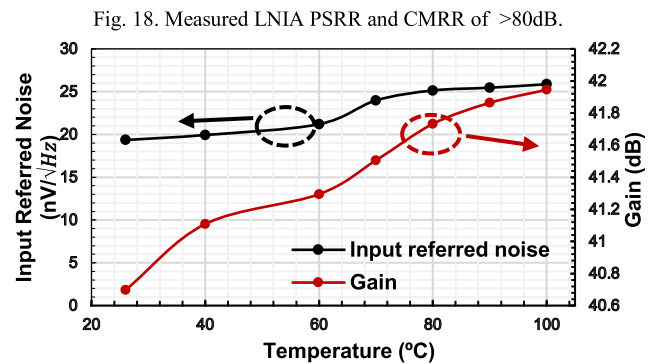
shown in Fig. 17(b). Fig. 18 shows the measured PSRR and CMRR. The measured values are greater than 80dB closer to DC and drop to 70 dB after 10Hz limited by the low bandwidth of the second-stage high gain amplifier. The CMRR is higher than 70 dB up to the interested bandwidth due to the wide-bandwidth first-stage preamplifier.
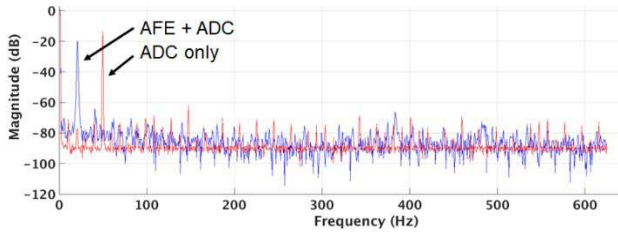
Fig. 20. Output spectrum of the signal path (blue) and ADC only (red). A 20 Hz tone is injected at the LNIA input and a 50 Hz tone is injected at the ADC input for testing.
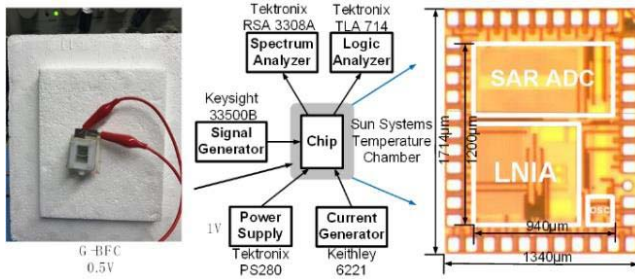

Fig. 21. Chip micrograph enabled by the external BFC supply.

Temperature stability is an important design parameter for IoT units stationed outside. The proposed switched-resistor biasing enables a PVT-stable operation at higher temperatures. This was verified using the proposed circuit (using bench supplies only) at temperatures up to 100°C. The chip was temperature cycled for validating stability performance and gain control. A gain and noise drift of only 0.039%/°C and 0.4%/°C have been measured as shown in Fig. 19.

The ADC was tested by applying a 50Hz single tone at the ADC input with LNIA disabled and the digitized output is captured by the logic analyzer to analyze the ADC output spectrum as shown by the red curve in Fig. 20. Fig. 20 further shows the performance of the entire signal path by capturing the digitized output spectrum (at the ADC output) with a 20Hz input tone applied to the LNIA input.

The amplitude of the input signal was divided by the gain of the LNIA to match the signal power in the ADC only measurement. There is a slight attenuation in the signal strength compared to the ADC only case mainly because of gain loss in the buffer stage. Table I compares the proposed work with recent state-of-art. The measured results in this work show superior noise-efficiency compared to the state-of-the-art, especially with the dual-supply solution. Future work will further enhance the energy-efficiencies through reduced-leakage design operating entirely at 0.5V. Fig. 21 shows the test setup with the die micrograph.

VI. Conclusion

This work demonstrates a long-term monitoring solution using enzymatic biofuel cell enabling a low-noise and temperature-stable analog front-end. Low-voltage robust design techniques with low-leakage and temperature-stable operation are demonstrated with more than 60% power savings using energy harvesting through BFC. Additionally, BFC-enabled AFE operates for more than 30 minutes without the need of any glucose replenishment. Our multipoint crosslink process ensures improved long-term stability of the BFC. The analog front-end uses a dual-supply LNIA with switched-resistor biasing to achieve the aforesaid energy efficiencies using a differential inverter-based preamp. The proposed system includes an on-chip split-DAC SAR-ADC and a single-opamp constant-charge subtraction relaxation oscillator consuming only $3.51\,\mu$W with the room-temperature NEF/PEF of 1.46 and 1.63 respectively. This work paves the path for the BFC to act as the sole energy source of perennial power replacing toxic batteries for implantable arterial models as well as wearable pain detection modules.

References

[1] A. Zebda *et al.*, "Single glucose biofuel cells implanted in rats power electronic devices," *Sci. Rep.*, vol. 3, Mar. 2013, Art. no. 1516.

[2] E. Romero, R. O. Warrington, and M. R. Neuman, "Energy scavenging sources for biomedical sensors," *Physiol. Meas.*, vol. 30, no. 9, pp. R35–R45, 2009.

[3] K. Wu, D. Choudhury, and H. Matsumoto, "Wireless power transmission, technology, and applications," *Proc. IEEE*, vol. 101, no. 6, pp. 1271–1275, Jun. 2013.

[4] M. H. Ouda, M. Arsalan, L. Marnat, A. Shamim, and K. N. Salama, "5.2-GHz RF power harvester in 0.18-μm CMOS for implantable intraocular pressure monitoring," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 2177–2184, May 2013.

[5] S. Ayazian, V. A. Akhavan, E. Soenen, and A. Hassibi, "A photovoltaic-driven and energy-autonomous CMOS implantable sensor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 336–343, Aug. 2012.

[6] J. Pan, B. Xue, and Y. Inoue, "A self-powered sensor module using vibration-based energy generation for ubiquitous systems," in *Proc. ASICON*, Oct. 2005, pp. 443–446.

[7] R. Sarpeshkar, *Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems*. Cambridge, U.K.: Cambridge Univ. Press, Feb. 2012.

[8] B. I. Rapoport, J. T. Kedzierski, and R. Sarpeshkar, "A glucose fuel cell for implantable brain–machine interfaces," *PLoS ONE*, vol. 7, no. 6, p. e38436, Jun. 2012.

[9] K. Niitsu, A. Kobayashi, Y. Ogawa, M. Nishizawa, and K. Nakazato, "An energy-autonomous, disposable, big-data-based supply-sensing biosensor using bio fuel cell and 0.23-V 0.25-μm zero-V$_{th}$ all-digital CMOS supply-controlled ring oscillator with inductive transmitter," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Oct. 2015, pp. 595–598.

[10] A. Kobayashi *et al.*, "Design and experimental verification of a 0.19 V 53 μW 65 nm CMOS integrated supply-sensing sensor with a supply-insensitive temperature sensor and an inductive-coupling transmitter for a self-powered bio-sensing system using a biofuel cell," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 6, pp. 1313–1323, Dec. 2017.

[11] S. Imani *et al.*, "A wearable chemical–electrophysiological hybrid biosensing system for real-time health and fitness monitoring," *Nature Commun.*, vol. 7, May 2016, Art. no. 11650.

[12] S. B. Calabrese, J. Gallaway, and P. Atanassov, "Enzymatic biofuel cells for implantable and microscale devices," *Chem. Rev.*, vol. 104, no. 10, pp. 4867–4886, Oct. 2004.

[13] J. Kim, H. Jia, and P. Wang, "Challenges in biocatalysis for enzyme-based biofuel cells," *Biotechnol. Adv.*, vol. 24, pp. 296–308, Jan. 2006.

[14] A. Galarneau *et al.*, "Synthesis of sponge mesoporous silicas from lecithin/dodecylamine mixed-micelles in ethanol/water media: A route towards efficient biocatalysts," *Microporous Mesoporous Mater.*, vol. 104, pp. 103–114, Aug. 2007.

[15] B. Willner, E. Katz, and I. Willner, "Electrical contacting of redox proteins by nanotechnological means," *Current Opinion Biotechnol.*, vol. 17, pp. 589–596, Dec. 2006.

[16] T. Garcia-Perez, S.-G. Hong, J. Kim, and S. Ha, "Entrapping cross-linked glucose oxidase aggregates within a graphitized mesoporous carbon network for enzymatic biofuel cells," *Enzyme Microbial Technol.*, vol. 90, pp. 26–34, Aug. 2016.

[17] M. Fischback *et al.*, "Enzyme precipitate coatings of glucose oxidase onto carbon paper for biofuel cell applications," *Biotechnol. Bioeng.*, vol. 109, no. 2, pp. 318–324, Feb. 2012.

[18] Micron Instruments. *DS-U-Shaped Gauges*. Accessed: Jul. 7, 2018. [Online]. Available: https://www.microninstruments.com/descriptions/productspecs/semiconductor_gages/DS-U-M_Semiconductor_Strain_Gage.pdf

[19] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[20] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV/$\sqrt{}$Hz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[21] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 μW 60 nV/$\sqrt{}$Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.

[22] R. Müller, S. Gambini, and J. M. Rabaey, "A 0.013 mm^2 5 μW DC-coupled neural signal acquisition IC with 0.5 V supply," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 302–304.

[23] K. A. Ng and Y. P. Xu, "A multi-channel neural-recording amplifier system with 90 dB CMRR employing CMOS-inverter-based OTAs with CMFB through supply rails in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[24] S. Song *et al.*, "A low-voltage chopper-stabilized amplifier for fetal ECG monitoring with a 1.41 power efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 237–247, Apr. 2015.

[25] H. Chandrakumar and D. Marković, "A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, Mar. 2017.

[26] F. M. Yaul and A. P. Chandrakasan, "A sub-μW 36 nV/$\sqrt{}$Hz chopper amplifier for sensors using a noise-efficient inverter-based 0.2 V-supply input stage," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 94–95.

[27] U. Ha *et al.*, "A 25.2 mW EEG-NIRS multimodal SoC for accurate anesthesia depth monitoring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 450–451.

[28] F. Zhang, J. Holleman, and B. P. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 344–355, Aug. 2012.

[29] T. C. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.

[30] J. A. Kaehler, "Periodic-switching filter networks-a means of amplifying and varying transfer functions," *IEEE J. Solid-State Circuits*, vol. SSC-4, no. 4, pp. 225–230, Aug. 1969.

[31] U. Denier, "Analysis and design of an ultralow-power CMOS relaxation oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1973–1982, Aug. 2010.

[32] H. Hu, S. Gupta, and M. Schiavenato, "An 143 nW relaxation oscillator for ultra-low power biomedical systems," in *Proc. IEEE Sensors*, Oct. 2016, pp. 1–3.

[33] S. Jeong, I. Lee, D. Blaauw, and D. Sylvester, "A 5.8 nW, 45ppm/°C on-chip CMOS wake-up timer using a constant charge subtraction scheme," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2014, pp. 1–4.

[34] J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," *IEEE J. Solid-State Circuits*, vol. SSC-10, no. 6, pp. 371–379, Dec. 1975.

[35] D. Gangopadhyay, E. G. Allstot, A. M. R. Dixon, K. Natarajan, S. Gupta, and D. J. Allstot, "Compressed sensing analog front-end for bio-sensor applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 426–438, Feb. 2014.

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