From Battery Enabled to Natural Harvesting: Enzymatic BioFuel Cell Assisted Integrated Analog Front-End in 130nm CMOS for Long-Term Monitoring

Huan Hu, Student Member, IEEE, Tanzila Islam, Alla Kostyukova, Su Ha, and Subhanshu Gupta∗, Senior Member, IEEE

Abstract— Biofuel cell as a natural energy source is a promising biocompatible technology which harvests the blood glucose into usable energy and replaces the toxic lithium-based battery solutions. However, the promise of this perennial non-toxic power is tempered by its unstable operation and low-voltage outputs leading to very limited operational lifetimes. This paper demonstrates a glucose-powered analog front-end with superior noise performance, which is enabled by standalone enzymatic biofuel cells operating for more than 30 min on active power without replenishment. Two biofuel cells are stacked to realize 0.5V output using commercially available glucose oxidase and the enzyme stability is improved via multipoint crosslinks by glutaraldehyde. To mitigate the effects of noisy and temperature-sensitive pseudo-resistors, a switched-resistor biasing scheme is applied to the input amplifier with the measured input-referred noise of 0.31 $\mu$V_RMS only. The proposed hybrid power scheme uses 1.6 $\mu$W from the battery with 1.9 $\mu$W provided by the biofuel cells. The entire analog front-end including a cascaded dual-supply amplifier with switched-capacitor SAR ADC and single-opamp relaxation oscillator occupies 1.12 mm². Measured results show on-chip gain and noise variations across temperature of only 1.1 dB and 19.2 nV/$\sqrt{\text{Hz}}$, respectively, with noise (power) efficient factor of 1.46 (1.63).

Index Terms— Natural energy harvesting, glucose bio-fuel cell, low-noise, low-power instrumentation amplifier, switched-resistor, split-DAC ADC, single-opamp relaxation oscillator.

I. INTRODUCTION

The emergence of ultra-low power analog processing techniques for bioelectronics in the past decade has deepened interests in sustainable power sources and energy scavenging systems for long-term monitoring and persistent sensing [1]–[7]. Biofuel cell for ultra-low-power CMOS devices is a promising biocompatible technology which harvests the blood glucose into usable energy and can replace the toxic lithium-based battery solutions. Compared to traditional batteries supplying each sensor node, the design of a biofuel cell (BFC) uses biocompatible enzyme-based electrodes (instead of expensive noble metal-based electrodes or toxic lithium ions) and can be a significant contributor towards future green nodes. Fig. 1 shows an approach towards future perennially powered enzymatic BFC-systems ‘producing’ usable energy on-demand from the body glucose and, ultimately, enabling unlimited functional lifetimes. Previous works have demonstrated the highest BFC potentials of around 0.2V-0.3V [8]–[11] with current outputs of a milli-Ampere. However, they exhibit poor long-term stability when loads are applied because the enzymes can be easily denatured and lose their catalytic functionality under various chemical and physical stresses imposed by the practical cell operating conditions. In this study, we present a contrasting approach with custom-designed stacked potential boosted BFC cells capable of micro-Ampere current output with an improved enzyme stability by introducing multipoint crosslinks.

We propose a low-noise sensitive microwatt front-end with superior noise- and energy-efficiencies using BFC to supplement the battery source while demonstrating operation for more than 30 minutes without any glucose replenishment. Section II describes briefly BFC construction methodology and design principles for long-term stability with manufacturing
steps. Section III describes the desired system specifications for a BFC enabled analog front-end (AFE) with a focus towards long-term monitoring. The limitation with low-current and low-voltage outputs from the BFC is overcome using a stacked voltage cell to realize an energy-efficient design of the AFE. Section IV illustrates the design techniques for the AFE with an on-chip relaxation oscillator and an analog-to-digital converter. Measurement results of the sensor front-end with BFC are presented in Section V, followed by conclusion and scope for future works in this exciting area in Section VI.

II. DEVELOPMENT OF ENZYME ELECTRODE-BASED BIOFUEL CELL AND ITS PERFORMANCE

Fig. 2 illustrates the working principle behind an enzymatic biofuel cell. It consists of three main components: an enzyme anode, an electrolyte, and an enzyme cathode. There are three principal enzyme electrode requirements for achieving high power density: 1) a high density of enzyme bound to the electrode surface, 2) a high electron transfer rate between the active site of the enzyme and the conductive electrode surface, and 3) a high mass transfer rate of reactants and products to and from the bound enzyme active sites [12]. While achieving all these requirements, the enzyme activity must be stabilized for the long-term operation to be achieved. To meet some of these requirements, various techniques have been developed by previous investigators to create functional BFC electrodes such as immobilizing the enzyme on the external surface of nanotubes, entrapping it in sol-gel or polymers, or chemically modifying structures of enzymes [13]–[15]. The typical BFCs suffer from their low reliability because the enzymes used to construct their electrodes can easily denature (i.e., die) by losing their unique tertiary structure under various external stresses (e.g., temperature, shear, pH, concentration, and pressure stresses). Unlike these conventional BFC designs, our current work in this manuscript fabricates the enzyme electrode using the unique Glucose Oxidase (GOx)-nanocomposite technique. This technique enhances the long-term stability of enzymes within the BFC electrode by forming the protein nanoparticles and encapsulating them within the mesoporous carbon network.

We used enzyme precipitation coating method to form GOx enzyme aggregates [11]. These GOx aggregates were entrapped by Graphitized Mesoporous Carbon (GMC) to form the GOx-nanocomposites as shown in Fig. 3(a) [16]. Our previous work suggests that nanocomposite structure offered both improved electrochemical performance and stability by combining the high electrical conductivity offered by the GMC network with the high enzyme loading and stability offered by the cross-linked GOx aggregates. Finally, the GOx-nanocomposites were used to prepare the anode enzyme electrode for the biofuel cell as shown in Fig. 3(b) [17]. Fig. 3(c) shows the assembled quarter-sized BFC. For this study, we only utilized the enzyme electrode design for the anode side of BFC to demonstrate our electrode design concept. However, we can apply a similar enzyme electrode design used for GOx for fabricating the cathode enzyme electrode using oxygen reducing enzymes (e.g., laccase). By integrating both anode and cathode enzyme electrode into well-established microfabrication technologies, one can design the complete BFC that could be implanted into the human blood vessel as shown in Fig. 1.

The total output power of BFC is dependent on the surface area of electrodes assuming there is no mass transfer limitation. As the surface area of the electrode increases, the number of the active site (i.e., the number of enzymes) increases. Assuming there are no mass transfer limitations of glucose fuels at the anode and oxygen from the air at the cathode, then these increased number of active sites should lead to increased power output as more glucose fuels can be oxidized for releasing increased numbers of electrons. In our design, the geometric surface area of the anode and cathode are about 0.332 cm².

III. DESIGN CONSIDERATIONS FOR ELECTRONIC SENSOR

This section describes the design considerations for interfacing the analog front-end (AFE) to the BFC. The focus of this work is to present efficiency enhancements using a low-voltage dual-supply low-noise instrumentation amplifier (LNIA) without any charge-pump action while achieving significant battery energy savings.

Simultaneously, it explores interoperability of the enzymatic biofuel cell with the CMOS electronics as illustrated in the
next section. Fig. 4 shows the system diagram of the proposed sensor front-end powered by the BFC measuring strain using a semiconductor piezoresistive sensor (PZR). The AFE comprises a dual-supply chopper-stabilized two-stage LNIA coupled to an on-chip temperature compensated relaxation oscillator (ROSC), a passive low-pass filter (LPF), and an intermediate driver stage followed by a low-input capacitance successive-approximation register analog-to-digital converter (ADC). The chopper stages in the LNIA and the ADC are clocked by the ROSC with an additional clock input (from the ROSC) feeding the biasing network for the LNIA. The BFC (0.5V) supplies the power-hungry stage in the LNIA and the rest is supplied by the battery (1V). Although the entire circuit can be energized only by the BFC, we chose to power the 1V supply with battery mainly because of the following reasons: 1) good power supply rejection ratio (PSRR) of the LNIA still needs to be maintained using a higher energy supply as there are no on-chip voltage regulators; 2) higher energy supplies can certainly be realized by stacking more number of BFCs, however, due to the current mismatch between individual cells, the output power efficiency might be degraded and thus reduce the operational times, and 3) combination of BFC and the battery creates two power domains such that the crosstalk between the oscillator, the ADC (typically noisy) and the LNIA can be reduced. Further research is still ongoing to completely eliminate battery without significant performance degradation.

Two off-chip highly sensitive PZR each of 10kΩ resistance and two on-chip poly resistors of equal resistance are connected in a Wheatstone Bridge configuration interfaced with the LNIA and attached to a flexible Tegaderm bandage to measure impedance changes due to strain as described in Section V. Semiconductor strain gages [18] are demonstrated to be more suitable for low noise strain sensing applications with a RMS noise floor of 0.04μV within a 1kHz bandwidth, which is 50× lower than foil strain gages. This corresponds to an integrated voltage noise of 3.5μVRMS within the 300Hz bandwidth. The noise from readout circuits thus cannot be neglected unless it contributes no more than 0.35μVRMS (based on the rule of thumb of 10 to 1 ratio). The voltage and strain relationship within the Wheatstone bridge configuration is shown as below:

\[ V = \varepsilon \times GF \times \frac{V_b}{2} \]

where \( \varepsilon \) is the strain applied, GF is the gage factor of the strain gage, and \( V_b \) is the voltage supply of Wheatstone bridge.

The full-scale output of the strain gage is calculated to be 1mV thereby required 45dB dynamic range (DR) with an 8-bit ADC.

IV. PROPOSED DUAL-SUPPLY LOW-NOISE ENERGY-EFFICIENT ANALOG FRONT-END

This section describes the design of the individual components of the AFE including LNIA, ROSC, and the ADC. Using low-voltage supply provided by the BFC, we first analyze the use of switched-resistors and its sensitivity to noise and temperature variation in comparison to pseudo-resistors.

A. Effects of Leakage and Temperature Sensitivity on Pseudo-Resistors in Comparison to Switched-Resistors

Past decade has seen wide usage of pseudo-resistor based capacitively-coupled LNIA in biophysiological signal monitoring applications [19]–[28]. As shown in Fig. 5, it comprises of an opamp (A) in a capacitive feedback network biased by GΩ pseudo resistors in subthreshold region with chopper stabilization stages [29]. Chopper stabilization is widely used to reduce the 1/f noise of the opamp and the DC offset to a first-order. An important consideration at low-supply
voltages is the second-order effect of the PVT-dependent bulk leakage in the pseudo-resistor that creates nonlinearity due to temperature sensitivity leading to significant resistance variation across temperature.

Pseudo resistors shown in Fig. 5, though an area efficient way to implement on-chip GΩ resistance based on their ultra-low subthreshold leakage currents suffer from the voltage swing dependent subthreshold leakage which tends to be highly non-linear. This limits the DR and noise sensitivity of the overall system. In addition, its subthreshold based leakage could vary by approximately 100× across temperature. The resistance of the pseudo resistors can be derived from the MOSFET subthreshold current equation,

\[ I_D = K \cdot V_T^2 \cdot \exp \left( \frac{V_{GS}}{nV_T} \right) \cdot \left[ 1 - \exp \left( \frac{-V_{DS}}{nV_T} \right) \right] \]  

(1)

where \( K \) is a device related parameter, \( V_T \) is the thermal voltage which equals to \( kT/q \), \( n > 1 \) is a nonideality factor. Differentiation by \( V_{DS} \) yields \( g_{ds} \):

\[ g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = K \cdot V_T \cdot \left[ \frac{1}{n} \cdot \exp \left( \frac{V_{DS}}{nV_T} \right) - \frac{(1-n)}{n} \cdot V_T \right. \]

\[ \left. \cdot \exp \left( \frac{(1-n) \cdot V_{DS}}{nV_T} \right) \right] \]  

(2)

which is exponentially proportional to \( V_{DS} \) from (2). Fig. 6 shows the simulated subthreshold leakage variation of a pseudo-resistor at room temperature against change in \( V_{DS} \).

Temperature dependency can also be derived by differentiating \( g_{ds} \) by temperature, written as below.

\[ \frac{\partial g_{ds}}{\partial T} = K \cdot \frac{1}{n} \cdot \left[ \frac{k}{q} \cdot \frac{V_{DS}}{nV_T} \cdot \exp \left( \frac{1}{n} \cdot \frac{qV_{DS}}{kT} \right) - (1-n) \cdot \frac{V_T}{n} \right. \]

\[ \left. \cdot \exp \left( \frac{(1-n) \cdot V_{DS}}{nV_T} \right) \right] \]

The above equation only considers the first-order temperature dependency of thermal voltage and ignores the second-order effects such as carrier mobility. Fig. 7 shows the simulated results of the temperature coefficient of pseudo-resistors with a constant \( V_{DS} \) of 100mV. A 215× incremental effective resistance from 100°C to 0°C yields a temperature coefficient of 2.15×/°C.

This PVT dependency of pseudo-resistors has limited the LNIA performance in high DR applications and systems operating under a wide range of temperatures. In this work, we replace the PVT-sensitive pseudo-resistors with switched-resistors implemented by a duty-cycled switch and a poly-resistor \( R_{poly} \) in series based on a periodic pulse switching system [30] shown in Fig. 8. The clock is directly coupled to on-chip low temperature-coefficient ROSC with an output pulse width duty-cycled at 2% [31]. The 2% duty-cycle is selected to avoid any dividers in the ROSC clock output and add more mismatch at higher power consumption. The LNIA is directly coupled to the buffered internal node of the ROSC as discussed further in Section IV.C. As the switch is driven by a pulsed clock with a duty cycle of \( D \), the effective resistance \( R_{eff} \) is boosted by 1/D given by \( R_{eff} = R_{poly}/D \). A large resistance can be implemented, especially in low frequency applications. The small duty cycle required can be easily realized with minimal circuit overhead as described in Section IV.

Obviating the need for any pseudo-resistors, this design leads to a temperature-stable implementation with low leakage. With a 2% duty-cycle clock, the \( R_{poly} \) that is used to implement the switched-resistor is about 1MΩ. The switched-resistor consumes an area of 20×20 μm² and is implemented with poly-resistors.

Interested readers can refer the seminal work by Kaehler [30] for the analysis of switched-resistors in both time and frequency domain and its impact to the LNIA noise. Chandrakumar [25] recently used Fourier transform to analyze the switched resistor circuits yielding an effective resistance:

\[ R_{eff_{switched}} = \frac{T}{T_d} \cdot R_{poly} = D \cdot R_{poly} \]

This change reduces the required passive resistance, \( R_{poly} \), by the duty-cycle factor. In our design, as the ROSC outputs a 2% duty-cycle clock, the effective resistance is observed to be amplified by 50×. In standard CMOS process, the temperature
coefficient of a poly-resistor can be as low as 500 ppm/°C while the pulse variation due to temperature in the ROSC is 20 ppm/°C, resulting in an overall temperature coefficient as low as 1%/°C which is approximately 200× better than the pseudo-resistors. Further improvements can be made using poly-resistors with positive- and negative-temperature coefficients. It is also significant to analyze the switched-resistors noise contribution as it is used in low-noise applications for most of the cases. The switched-resistor operates as a sample-and-hold circuit similar to switched-capacitor circuits. The noise contributed by the effective resistance $R_{\text{eff}}$ being sampled on the capacitor has a power spectral density of $4kTR_{\text{eff}}$ with a bandwidth determined by $R_{\text{eff}}$ and $C_{\text{par}}$. Therefore, the total noise contributed by switched-resistors, $kT/C_{\text{par}}$, is the same as in sample-and-hold. Thus, in order to minimize the noise floor of a switched-resistor, a large sampling capacitor is still required.

B. Proposed Two-Stage Dual-Supply BFC-Enabled LNIA

1) Semi-Pseudo-Differential 1st Stage Preamp: Recent state-of-the-art LNIA’s have employed two-stage dual-supply amplifiers for demonstrating higher noise- and power efficiencies. The low-noise current-hungry first stage preamplifier operated at low supply voltages followed by a high-noise low-power second stage amplifier operating with a high supply voltage breaks the trade-off between power-efficiency and noise-efficiency. Yaul and Chandrakasan [26] recently demonstrated a two-stage LNIA with a 0.2V pseudo-differential first stage biased using pseudo-resistors and a high-gain second-stage amplifier. The two-stage dual supply topology realized low-noise with good power efficiency and common-mode rejection ratio (CMRR) using beyond-rail biasing. However, a low-pass corner formed by pseudo-resistor in the common-mode feedback loop leads to a frequency dependent pole that results in poor settling. For applications using aggressive duty-cycling, this turn-ON time adversely limits the overall performance. The pseudo-differential design further limits the PSRR thus on-chip switching regulators are implemented at the cost of power and area overhead. Chandrakumar and Marković [25] replaced pseudo-resistors by switched-resistors. However, without any on-chip clock generator, the generation of nanosecond pulses is susceptible to process variations requiring manual calibration steps.

In this work, a two-stage dual-supply chopper-stabilized LNIA topology is used. The first-stage current-intensive preamplifier is powered up by the BFC with the second stage amplifier still enabled by the battery. This arrangement enables more than 60% savings in power and saves precious battery resources limited currently by the BFC. While future implementations of BFC will enable replacing the battery completely, this work illustrates superior noise- and power-efficiencies using this dual-supply feature.

In Fig. 9(a), the proposed LNIA followed by a passive RC LPF and a driver stage. The entire cascaded two-stage amplifier is capacitively coupled with an embedded chopper stabilization stages. The chopping frequency is selected to be 20kHz (twice the flicker noise corner frequency) generated from the on-chip nanowatt ROSC which will be discussed later. $V_{\text{bias}}$ is generated on-chip to bias the PMOS devices inside the first-stage preamplifier through a large resistor $R_{\text{bias1}}$. $C_{\text{par1}}$ together with $R_{\text{bias1}}$ forms a high-pass filter whose corner frequency is set one order of magnitude smaller than the chopped input signal frequency (20kHz) to avoid any attenuation to the input signal. $R_{\text{bias1}}$ and $C_{\text{par1}}$ are chosen to be 50Ω and 10pF respectively, forming a high pass frequency at around 300Hz. Therefore, $C_{\text{f}}$ is set to be 100fF to achieve a closed loop gain of 40dB.

Fig. 9. (a) Proposed two-stage chopper-stabilized low-power, low-noise LNIA with passive filter and a buffer for off-chip drive, (b) detailed circuit diagram of the 1st stage preamp with switched-resistor biasing, (c) signal flow diagram of the proposed pre-amplifier, (d) single-ended representation of the proposed LNIA, and (e) on-chip reference generator using stacked PMOS diodes.
We illustrate a semi-pseudo differential inverter-based preamplifier enabled by the 0.5V BFC without any supply boosting. The pseudo-differential design with the tail current source ensures enough headroom on each transistor as shown in Fig. 9(b) while drawing 4.26μA in the simulation. The current reuse scheme enabled by the input complementary differential pairs approximately doubles the effective transconductance of the amplifier which consequently halves the input-referred noise. The output common mode voltage is set by an error amplifier (EA) to \(V_{\text{cm1}}\) through a feedback loop by controlling the gate bias voltage of \(M_{p1}\) DC coupled by a large resistor \(R_{\text{bias2}}\) implemented with the switched-resistor described in Section IV.A. Each of the EAs are chopper stabilized in the common-mode signal path and hence, do not contribute any additional offsets or flicker noise to the preamplifier input while consuming only 20 nW power. A preamp tail current source \((M_{q2})\) with temperature-compensated gate bias is used to enhance CMRR across temperature while reducing the effect of supply spurs. The tail current source reduces the effect of supply spurs compared to [26]. \(C_{\text{AC}}\) decouples the gate DC bias of \(M_p\) and \(M_{n1}\) to add an extra degree of freedom in the design.

From the single-ended representation of the pre-amplifier shown in Fig. 9(d), the input voltage \(V_{\text{in}}\) is directly coupled to the gate of \(M_p\) while it is AC coupled to the gate of \(M_{n1}\) through \(C_{\text{AC}}\). \(C_{\text{AC}}\) forms a capacitive divider with \(C_{\text{par2}}\), the parasitic capacitor at the gate of \(M_{n1}\). The small signal voltage at the gate of \(M_p\) can be written as:

\[
V_{g,n1} = \frac{C_{\text{AC}}}{C_{\text{AC}} + C_{\text{par2}}} \cdot V_{\text{in}}
\]

From the above, \(C_{\text{AC}}\) has to be large enough compared to \(C_{\text{par2}}\) to avoid any input signal attenuation. Biased in weak inversion for maximum \(g_{m}\) efficiency at the same current density level, the size of the input devices \((M_p, M_{n1})\) are typically large which makes its parasitics not negligible. Thus, we choose \(C_{\text{AC}}\) to be 5pF. Observing the feedback loop, there are two critical nodes in the pre-amplifier which creates a pole at the inverter output, and at the gate of \(M_{n1}\) (Fig. 9(d)). The inverter stage burns a large amount of current to reduce the noise floor, pushing the pole at its output far outside the bandwidth to be a non-dominant pole. The pole at the gate of \(M_{n1}\), due to the large effective resistance of the switched resistor \(R_{\text{bias2}}\) and the large AC coupling capacitor, \(C_{\text{AC}}\) (as discussed above to ensure no signal attenuation), becomes the dominant pole and is typically well separated from the non-dominant pole. The stability of the loop thus won’t be a major concern even without compensation. However, the dominant pole at the gate of \(M_{n1}\) severely affects settling and slow down the system transient response, especially in low power applications where the circuits can be aggressively duty-cycled. Therefore, it is essential to analyze the loop’s frequency response. The feedback voltage, \(V_{fb}\) can be obtained by breaking the loop at the gate of \(M_p\) as follows:

\[
V_{fb} = \left( g_{m,M_p}V_{in} + g_{m,M_{n1}}V_{fb} \right) \left( \frac{R_{\text{out}}}{1/sC_L} \right) A \cdot \beta
\]

(3)

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\[
\beta = \frac{1}{sC + R_{\text{bias2}}} = \frac{1}{1 + sR_{\text{bias2}}C}
\]

\[
C = \left( \frac{1}{sC_{\text{par1}}} + \frac{1}{sC_{\text{AC}}} \right) / \left( \frac{1}{sC_{\text{par2}}} \right)
\]

\[
R_{\text{out}} = \frac{r_{o,Mp}}{r_{o,Mn1}}
\]

where \(g_{m,Mp} (r_{o,Mp})\) and \(g_{m,M_{n1}} (r_{o,Mn1})\) are the transconductance and output resistance of \(M_p\) and \(M_{n1}\) respectively. \(C_L\) is the load capacitance at the inverter output, \(A\) is the DC gain of the EA and \(C_{\text{par1}}\) is the parasitic capacitance at the gate of \(M_p\). From (3), the loop gain is derived as:

\[
LG = \frac{V_{fb}}{V_{in}} = \frac{g_{m,Mp} \cdot (R_{\text{out}} / \left( \frac{1}{sC_L} \right)) \cdot A \cdot \beta}{1 - g_{m,M_{n1}} \cdot (R_{\text{out}} / \left( \frac{1}{sC_L} \right)) \cdot A \cdot \beta}
\]

(5)

Substituting (4) into (5) we can get

\[
LG = \frac{g_{m,Mp}R_{\text{out}}A}{s^2R_{\text{bias2}}C^2 + s\left( R_{\text{bias2}} + R_{\text{out}} \right) C + 1 - g_{m,M_{n1}}R_{\text{out}}A}
\]

From above, the feedback loop forms a two-pole low-pass characteristic. For fast settling, the combination of \(C_{\text{AC}}\) and \(R_{\text{bias2}}\), \(C_{\text{par1}}\) and \(C_{\text{par2}}\) cannot be too large. \(C_{\text{AC}}\) is set to 5pF as discussed above, thus \(R_{\text{bias2}}\) needs to be well-controlled to maintain an acceptable loop bandwidth and hence settling time across corners and temperatures. The merit of switched-resistors plays an important role in implementing \(R_{\text{bias2}}\). As discussed in Section IV.A, the resistance of pseudo-resistors can vary up to 200× from 0°C to 100°C, which directly changes the loop bandwidth by 200× proportionally. This severely limits the duty cycle of the overall system in ultra-low power applications. Fig. 10 shows the simulated loop bandwidth with respect to different \(R_{\text{bias2}}\) values from 1MΩ to 200MΩ to mimic the 200× incremental effect in the resistance of pseudo resistor from 100°C to 0°C, observing a decrease in loop bandwidth over 200×. Substituting the pseudo-resistor with switched-resistor, the incremental effect can be minimized thus creating a PVT constant settling behavior. In our design, \(R_{\text{bias2}}\) is set to 50 MΩ. Fig. 9(c) shows the signal flow diagram of the proposed pre-amplifier. Though the EA will feedback its own noise to input, \(R_{\text{bias2}}\) together with \(C\) forms a low pass filter in the feedback path which greatly limits the noise bandwidth of the EA. The EA has negligible in-band noise contribution and the only active component that contributes to noise is the inverter-based amplifier. The inverter-based input complementary pairs are biased in weak inversion region to maximize its transconductance efficiency while drawing large current to reduce the input-referred noise voltage. Operating at 0.5V, it can draw 2× current while still maintaining the same power consumption. Flicker noise, mismatch and offset at the preamplifier input in the differential signal path is mitigated through the chopper-stabilization stage at the input capacitor (coupled to the PZR) and the preamp output. The decoupling capacitor \((C_{\text{AC}})\) used between \(M_{n1}\) and \(M_p\) allows an extra degree of freedom to bias the preamp inputs.

All the reference voltages are generated on-chip. As the accuracy and line sensitivity is not a major concern here as long as all the transistors can operate with enough headroom, the references are generated using stacked-PMOS diodes in
maximizing the transconductance. The overall input referred noise of the LNIA is approximately,

\[
\frac{v_n^2}{\Delta f} = \left( \frac{C_s + C_f}{C_s} \right)^2 \left[ \frac{4kT\gamma}{g_m,M1 + g_m,Mp} \right] + \frac{g_m,M1 \left( g_m,M1 + g_m,Mp \right)^2 \left( \frac{1}{r_o,M1} + \frac{1}{r_o,Mp} \right)^2}{8g_m,M1 \left( g_m,M1 + g_m,Mp \right)^2 \left( \frac{1}{r_o,M1} + \frac{1}{r_o,Mp} \right)^2} \]

where \( g_m,M1 \) is the transconductance of second stage input differential pair, \( g_m,M3 \) and \( g_m,M6 \) is the transconductance of the two current sources of the folded-cascode amplifier respectively.

### C. On-Chip Nanowatt Relaxation Oscillator Using Single-Opamp Constant Charge Subtraction

Relaxation oscillators (ROSC) are increasingly being used as a clock reference due to their low-power operation and ease of on-chip integration in standard CMOS processes [31]. In this section, we expand our recent work [32] using a single-opamp switched-current amplifier with constant charge subtraction technique which is proposed in [33] as shown in Fig. 13. The principle of operation is explained as below.

Assuming an initial condition when \( C_1 \) is fully discharged, the comparator, \( Comp_1 \), outputs a low setting the output of the R-S latch as \( \Phi_1 = 1 \) and \( \Phi_2 = 0 \). During \( \Phi_1 = 1 \), \( C_1 \) is charged by a constant current source, and \( C_2 \) is charged through a constant voltage source to a fixed voltage with the op-amp shorted. The comparator switches its state after \( C_1 \) is charged exceeding the \( Comp_1 \) threshold, \( V_{th1} \). The output phases are now \( \Phi_1 = 0 \) and \( \Phi_2 = 1 \). During \( \Phi_2 = 1 \), \( C_2 \) is connected in feedback across the op-amp resulting in charge subtraction between \( C_2 \) and \( C_1 \). A constant charge will always be subtracted on \( C_1 \) during every cycle when \( \Phi_2 \) is enabled as shown in Fig. 13. By charge conservation,

\[
C_1 V_{th1} - C_2 V_{ref} = C_1 V
\]

where \( V_{th1} \) is the comparator threshold voltage, \( V_{ref} \) is the subtracted voltage and \( V_{C1} \) is the input voltage of the comparator. Thus,

\[
V_{C1} = V_{th1} - \frac{C_2}{C_1} V_{ref}
\]

Therefore, as a constant voltage \( V_{ref} \) is subtracted from \( V \). The resulting oscillating frequency is shown in (8) assuming \( C_1 \) and \( C_2 \) are equal.

\[
f_{osc} = \frac{I_{ref}}{C_1 V_{ref}}
\]
the circuit operation with the op-amp reference current supply being switched between two different current sources. The low power mode is enabled during \( \Phi_1 \) to help preset the initial DC operating point and the high-power fast-settling mode is enabled during \( \Phi_2 \) to accurately realize the charge subtraction. The settling time required in \( \Phi_2 \) is shown in (9), where \( g_m \) is the effective trans-conductance of the op-amp and \( \varepsilon \) is the settling error.

\[
t_s = \frac{C_1}{C_2} \ln(\varepsilon) \frac{g_m}{g_m} \quad (9)
\]

A two-stage amplifier topology is chosen here due to a large input common mode range and output swing since the op-amp needs to tolerate a large swing at both the input and output (Fig. 13). Further discussion on flicker and thermal noise constraints can be obtained from [32]. Fig. 14 shows the simulated phase noise from the relaxation oscillator and it’s temperature stability when operating at the 20kHz oscillation frequency. Both the 2%/50% duty-cycle clock outputs are generated by the described circuit without any additional overhead and are used to activate the switched-resistor in the LNIA, the chopper switches, and the SAR-ADC.

D. Differential C-2C/Binary DAC Based SAR-ADC

An 8-bit differential successive approximation analog-to-digital converter (SAR-ADC) (Fig. 15) is implemented following the proposed LNIA and a second-order passive low-pass filter. The performance of the ultra-low-power subthreshold
ADC has been limited by the thermal noise and the input offset of the comparator. Conventional binary-DACs [34] with effective input capacitance ($= 2^n C_u$) occupies a large area and suffers from charge injection ($C_u$ is the unit capacitor in the DAC). In contrast, the C-2C DAC structure [35] reduces the effective input capacitance to $2C_u$. The C-2C DAC architecture however suffers from poor matching and linearity. In our design, we chose a hybrid split-DAC structure with a 4-bit C-2C DAC (LSB) and a 4-bit binary DAC (MSB), resulting in lower input capacitance of $2^n/2 + 1 C_u$. The unit capacitor is selected to be $77 \mu F$ with an 8-bit DAC based on the thermal noise floor limitation, $\sqrt{kT C} < \frac{1}{2} \cdot \frac{1}{n} \cdot V_{in}$, where $V_{in}$ is the full-scale input signal.

The comparator preamplifier has an input-offset cancellation circuit to alleviate the flicker noise and the offset. By connecting the preamplifier in unity-gain feedback during the sampling phase, the offset voltage of the preamplifier is sampled and subtracted in the next phase, resulting in an effective offset voltage of $V_{os}/A$, where $V_{os}$ is the preamplifier offset voltage and $A$ is the preamplifier gain. The input differential devices are sized to be $60 \mu m/1 \mu m$ to further reduce the mismatch and flicker noise. The comparator as the only component that consumes static power has a power consumption of only 120nW. The buffer in between the LNIA and ADC provides isolation from clock feedthrough and kickback on the LNIA output.

V. MEASUREMENT RESULTS

The readout sensor IC is interfaced with a sensitive semiconductor PZR (gage factor = $175 \pm 10$) manufactured by Micron Instruments. With the input chopper-stabilization, the LNIA input impedance at $5 M\Omega$ is sufficiently larger than the $10 k\Omega$ impedance of the PZR for this application avoiding loading effects. Fig. 16(a) shows the measured differential outputs of the readout sensor IC when interfacing with the BFC. A gain of around 100 is observed with an input of 1 mVpk-pk sine signal at the LNIA input meeting the design target of 40 dB. Fig. 16(b) further shows the response of the BFC when loaded. The BFC can provide a stable standalone output voltage for more than 30 min. This can be further extended with continuous glucose replenishment. The readout sensor IC was fabricated in 0.13$\mu$m CMOS technology with an active area of 1.12$mm^2$ without pads. The active area without pads and decap is 0.8$mm^2$ including LNIA, ADC, and ROSC. The dual-supply scheme with two power sources provides greater than 60% energy savings. The 0.5V BFC supply provides 1.9$\mu W$ with the rest 1.61$\mu W$ supplied by the 1V battery. Fig. 17(a) shows the measured LNIA gain frequency response at the output of
Table I: Comparison of BFC Enabled AFE+ADC with State-of-the-Art

<table>
<thead>
<tr>
<th></th>
<th>[24]</th>
<th>[25]</th>
<th>[26]</th>
<th>[27]</th>
<th>[28]</th>
<th>This work</th>
</tr>
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<tbody>
<tr>
<td>Process/Publication</td>
<td>180 nm BTicAS’15</td>
<td>40 nm JSSC’17</td>
<td>180 nm ISSCC’16</td>
<td>65nm ISSCC’17</td>
<td>130 nm/500 nm BTicAS’12</td>
<td>130 nm</td>
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<tr>
<td>Supply (V)</td>
<td>0.3/0.6/1.2 (Batt)</td>
<td>1.2 (Batt)</td>
<td>0.2/0.8 (Batt)</td>
<td>1.2 (Batt)</td>
<td>1 (Batt)</td>
<td>0.5 (BFC) / 1 (Batt)</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>1.6 (LNIA/LDO/CP/Buffer)</td>
<td>0.071 (LNIA only)</td>
<td>1 (LNIA/PGA/AAF)</td>
<td>16 (System)</td>
<td>0.047/0.046/0.072 (LNIA only)</td>
<td>0.44 (AFE) 1.12 (Total)</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>33</td>
<td>26</td>
<td>57.8</td>
<td>40</td>
<td>40.5/36.1/40</td>
<td>40</td>
</tr>
<tr>
<td>BW (Hz)</td>
<td>0.7-182</td>
<td>200/5000</td>
<td>670</td>
<td>250</td>
<td>0.4-8.5k/0.3-4.7k/0.05-10.5k</td>
<td>300</td>
</tr>
<tr>
<td>IRN (nV/√Hz)</td>
<td>24.4</td>
<td>80 @ 200 Hz</td>
<td>36 (0.5-670)</td>
<td>–</td>
<td>–</td>
<td>19.2 @ 100 Hz</td>
</tr>
<tr>
<td>Integr. IRN (uVRms)</td>
<td>0.34/1.01</td>
<td>2 (1-200 Hz) 7 (200-5000Hz)</td>
<td>0.94 (0.670 Hz)</td>
<td>0.44 (0.5-100)</td>
<td>3.2/3.6/2.2 (1-300 Hz)</td>
<td>0.31</td>
</tr>
<tr>
<td>Gain drift across temp (%/°C)</td>
<td>–</td>
<td>–</td>
<td>0.7 @ 100 Hz*</td>
<td>–</td>
<td>–</td>
<td>0.4 @ 100 Hz</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>&gt;70</td>
<td>-</td>
<td>85</td>
<td>&gt;110</td>
<td>60/-80</td>
<td>92</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>&gt;70</td>
<td>-</td>
<td>80</td>
<td>60/5.5/-80</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td>Power (μW)</td>
<td>1.17/0.3</td>
<td>2 (Batt)</td>
<td>0.79 (Batt)</td>
<td>5.4</td>
<td>12.5/0.8/12.1</td>
<td>1.9 (GBFC) 1.61 (Batt)</td>
</tr>
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<td>NEF/PEF [1]</td>
<td>1.74/1.05</td>
<td>4.9/7</td>
<td>2.1/1.6</td>
<td>3.5/-</td>
<td>4.5/1.9/2.9/-</td>
<td>1.46/1.63</td>
</tr>
<tr>
<td>Blocks</td>
<td>LNIA/LDO/Charge pump/Buffer</td>
<td>LNIA only</td>
<td>LNIA/PGA/AAF [2]</td>
<td>System-on-Chip</td>
<td>LNIA only</td>
<td>LNIA/Buffer/ADC/ROSC</td>
</tr>
</tbody>
</table>

\[ \text{NEF} = \frac{V_{\text{rms}}}{\sqrt{2V_{\text{total}} / (2N+1)T+V_{\text{BW}}} \times P_{\text{total}} \times V_{T} - \text{Thermal Voltage}} \]

\[ \text{PEF} = \frac{2V_{\text{rms}}}{\sqrt{2V_{\text{total}} / (2N+1)T+V_{\text{BW}}} \times P_{\text{total}}} \]

* Estimated \[ \text{PGA} - \text{Programmable Gain Amplifier, AAF - Anti-Aliasing Filter} \]

Fig. 18. Measured LNIA PSRR and CMRR of >80dB.

Fig. 19. Measured LNIA gain and input-referred noise with temperature variation from 25-100°C.

the off-chip buffer with a loading capacitor of 47nF in order to limit the bandwidth due to the high-current low-noise design of the first stage preamplifier. The measured gain profile shows a droop at 200Hz due to extra package parasitics. The response shows a single-pole response of 20dB/decade between 300Hz-10kHz.

An input-referred noise density of only 19.1nV/√Hz is measured at 100Hz with the total integrated input-referred noise in the 1-300Hz bandwidth measured to be 0.31μVrms as shown in Fig. 17(b). Fig. 18 shows the measured PSRR and CMRR. The measured values are greater than 80dB closer to DC and drop to 70 dB after 10Hz limited by the low bandwidth of the second-stage high gain amplifier. The CMRR is higher than 70 dB up to the interested bandwidth due to the wide-bandwidth first-stage preamplifier.
Temperature stability is an important design parameter for IoT units stationed outside. The proposed switched-resistor biasing enables a PVT-stable operation at higher temperatures. This was verified using the proposed circuit (using bench supplies only) at temperatures up to 100°C. The chip was temperature cycled for validating stability performance and gain control. A gain and noise drift of only 0.039%/°C and 0.4%/°C have been measured as shown in Fig. 19.

The ADC was tested by applying a 50Hz single tone at the ADC input with LNIA disabled and the digitized output is captured by the logic analyzer to analyze the ADC output spectrum as shown by the red curve in Fig. 20. Fig. 20 further shows the performance of the entire signal path by capturing the digitized output spectrum (at the ADC output) with a 20Hz input tone applied to the LNIA input.

The amplitude of the input signal was divided by the gain of the LNIA to match the signal power in the ADC only measurement. There is a slight attenuation in the signal strength compared to the ADC only case mainly because of gain loss in the buffer stage. Table I compares the proposed work with recent state-of-art. The measured results in this work show superior noise-efficiency compared to the state-of-the-art, especially with the dual-supply solution. Future work will further enhance the energy-efficiencies through reduced-leakage design operating entirely at 0.5V. Fig. 21 shows the test setup with the die micrograph.

VI. CONCLUSION

This work demonstrates a long-term monitoring solution using enzymatic biofuel cell enabling a low-noise and temperature-stable analog front-end. Low-voltage robust design techniques with low-leakage and temperature-stable operation are demonstrated with more than 60% power savings using energy harvesting through BFC. Additionally, BFC-enabled AFE operates for more than 30 minutes without the need of any glucose replenishment. Our multipoint crosslink process ensures improved long-term stability of the BFC. The analog front-end uses a dual-supply LNIA with switched-resistor biasing to achieve the aforesaid energy efficiencies using a differential inverter-based preamp. The proposed system includes an on-chip split-DAC SAR-ADC and a single-opamp constant-charge subtraction relaxation oscillator consuming only 3.51μW with the room-temperature NEF/PEF of 1.46 and 1.63 respectively. This work paves the path for the BFC to act as the sole energy source of perennial power replacing toxic batteries for implantable arterial modules as well as wearable pain detection modules.

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REFERENCES


Huan Hu (S’17) received the B.S. degree in electrical engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2012, and the M.S. degree from Oregon State University, Corvallis, OR, USA, in 2015. He is currently pursuing the Ph.D. degree in electrical engineering at Washington State University, Pullman, WA, USA. He held a design intern position with Micro System Engineering, Lake Oswego, OR, USA, in Fall 2018. His research interests include ultra-low-power sensor interface designs, clock generation, and subthreshold circuit designs.

Alla Kostyukova received the B.S./M.S. degrees from Saint Petersburg State University, Russia, and the Ph.D. degree from the Institute of Protein Research/Moscow State University, Russia. She is currently an Associate Professor with the Gene and Linda Voiland School of Chemical Engineering and Bioengineering, Washington State University. She has advised three M.S. graduates, six Ph.D. graduates, and two post-doctoral fellows. She has published more than 55 papers with h-index of 21.

Su Ha received the B.S. degree from North Carolina State University, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana–Champaign. Since 2005, he has been the Director for O.H. Reaugh Laboratory for Oil and Gas Processing, Washington State University. From 2013 to 2014, he was an International Scholar at Kyung Hee University, South Korea. He is currently a Professor with the Gene and Linda Voiland School of Chemical Engineering and Bioengineering, Washington State University.

He has advised approximately four M.S. graduates, 13 Ph.D. graduates, and three post-doctoral fellows. He has published more than 70 papers with h-index of 28, and received several awards for outstanding teaching and research, including the 2008 and 2017 Outstanding Teaching Awards for the Voiland School at Washington State University, the 2014 Highly Cited Researcher Award from Thomson Reuters, and the 2014 Brain Pool Award from Korea Science and Engineering Foundation.

Subhanshu Gupta (S’03–M’11–SM’16) received the B.E. degree from the National Institute of Technology, Trichy, India, in 2002, and the M.S. and Ph.D. degrees from the University of Washington in 2006 and 2010, respectively. He was with Maxim-ic, National Semiconductor and Novell Netware in research and development positions. He is currently an Assistant Professor at the School of Electrical Engineering and Computer Sciences, Washington State University. His research interests include preserving interface designs, clock generation, and subthreshold circuit designs. He was a recipient of the Analog Devices Outstanding Student Designer Award in 2008 and the IEEE RFIC Symposium Best Student Paper Award in 2011.