A 0.22-μW Single-Bit VCO-Based Time-Domain Sensor-to-Digital Front-End With Reduced Supply Sensitivity

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***Abstract*— Future energy harvesting systems require ultra-low supply sensor interfaces operating at sub-0.4 V. Time-based sensor-to-digital interfaces, though compatible with ultra-low supply, are highly sensitive to inherent mismatch in the current-controlled ring oscillators (CCRO) especially in a multi-bit architecture. Contrary to a multi-bit sensor interface, this work realizes a single-bit system replacing the multi-phase CCRO with a nanoWatt current-controlled relaxation oscillator (CCRxO) and thus obviating the significant delay cell mismatch in the CCROs. In addition, we propose a time domain calibration loop (TDCL) to mitigate the high signal-to-noise and distortion ratio (SNDR) sensitivity related to the K_{VCO} variation with respect to supply. A pulse-biasing circuit is proposed for fast settling of the internal nodes and facilitate quick switching between calibration and data conversion modes. The proposed closed-loop single-bit VCO-based sensor-to-digital front-end with TDCL was fabricated in 180 nm CMOS technology. Operating under 0.35 V, the chip consumes a total power consumption of 0.22 μW only with a SNDR of 63.2 dB. The SNDR variation is measured to be only 1.7 dB with more than 50% supply variation validating the effectiveness of the proposed TDCL.**

***Index Terms*— VCO-based sensor-to-digital front-end, ultra-low supply, low-leakage circuits, time-domain offset calibration, fast pulse-biasing.**

I. Introduction

ENERGY harvesters, as the replacement of conventional batteries in the future micro-sensing systems, are able to collect energy in various forms from the surroundings and convert into electricity. However, the scavenged energy randomly depends on the environment and use conditions which tends to be unreliable. Additionally, the open circuit (OC) voltage (<0.5 V) of most of the energy harvesters are quite limited as evident in Fig. 1(a) [1]–[4]. State-of-the-art energy harvesting systems thus rely on DC-DC converters and power management units [5] to provide a well-regulated supply for CMOS electronics to survive.

Recent works on ultra-low-supply sensor interfaces have offered tremendous opportunity to run directly with energy harvesters without any DC-DC converters. Further merging the front-end amplifier with the analog-to-digital converter (ADC) and realizing a noise shaping direct sensor-to-digital front-end (SD-FE) has created significant power and area savings [6]–[9]. Fig. 1(b) summarizes the recent state-of-the-art sub-0.5 V worksincluding both $\Delta\Sigma$-ADC and direct SD-FE that can be potentially integrated into an energy harvesting system. From Fig. 1(b), it is evident that these works fall into three major categories: (i) inverter-based integrator [10]–[17], (ii) passive integrator [18], [19], and (iii) voltage-controlled oscillator (VCO)-based integrator [20]–[25]. Even though the inverter-based architecture can achieve higher signal-to-noise and distortion ratio (SNDR) using higher orders of

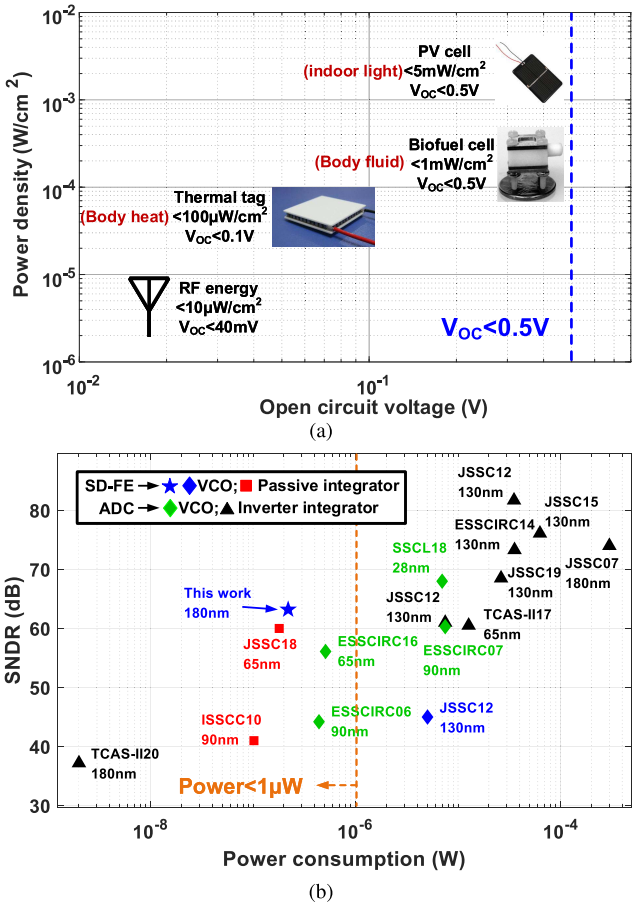

Fig. 1. (a) Power density and open circuit voltage range of various energy harvester that can be potentially integrated into a wearable or implantable sensor, and (b) survey on power consumption vs. SNDR of $\Delta\Sigma$ ADC and SD-FE under sub-0.5 V supply (2006-2020).

Manuscript received March 7, 2021; revised June 22, 2021; accepted July 7, 2021. This work was supported in part by the National Science Foundation CAREER under Award 1944688 and in part by the Washington Research Foundation (WRF). This article was recommended by Associate Editor J. Lota. *(Corresponding author: Huan Hu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2021.3096838.

Digital Object Identifier 10.1109/TCSI.2021.3096838

noise shaping, multi-stage opamps are required to realize a high open loop gain which increases power consumption. The passive-integrator architecture demonstrates comparable SNDR with reasonable power consumption. Yet the passive elements are sensitive to PVT variation and can hardly maintain stable performance. In contrast, the VCO-based integrator benefits from the time-domain nature and digital-intensive architecture, and hence it has the potential to achieve high signal-to-quantization noise ratio (SQNR) at ultra-low supply voltage. Moreover, it readily scales with CMOS technology yielding energy and area efficient design.

Among the VCO-based approaches, the single-bit quantization benefits from smaller propagation delays in the critical path at ultra-low supply voltage [25] as compared to multi-bit designs. However, this degrades the system energy efficiency as the ring-oscillator (RO) based single-bit $\Delta\Sigma$ modulator does not use the inherent multi-phase RO outputs [20], [25], [26]. Additionally, the VCO gain, K_{VCO}, is highly supply dependent negatively impacting the SQNR variation. Prior work in [24] used a self-compensated current reference to mitigate the VCO current variation. Nevertheless, a 16-bit trimming is still required to deal with the local mismatch. A resistive digital-to-analog converter (R-DAC) was introduced at the input in [25] to tune the V-F characteristic of the VCO. However, the R-DAC tuning for each supply point makes it inefficient and cumbersome. The R-DAC further reduces the input impedance while adding input-referred noise, which makes it infeasible to directly interface with the sensor.

To address the aforementioned issues, this work proposes a sub-0.4V VCO-based single-bit SD-FE architecture including: (i) a nanowatt relaxation oscillator (RxO) replacing the RO to enable single-bit operation followed by (ii) the necessary digital blocks for frequency-to-digital conversion, (iii) a cost-efficient time-domain calibration loop (TDCL) to ensure robust operation over supply variation, and (iv) a pulse-biasing technique for fast switching between calibration and data conversion modes. Benefited from the digital-intensive architecture and time-domain nature, the SD-FE directly operates under sub-threshold supply voltage. With the assistance of the TDCL, the SD-FE SNDR performance variation is significantly reduced over a wide range of supply variation without any power management unit.

The rest of the paper is organized as follows. Section II briefly introduces the VCO-based SD-FE and analyzes the linearity of the RO and the RxO operating at ultra-low supply voltage. Section III describes the system design considerations of the proposed single-bit VCO-based SD-FE. Section IV presents the detailed circuit implementation including the VCO, clock boosting circuits, TDCL and the pulse biasing technique. Section V presents the measurement results followed by conclusions and future research directions in Section VI.

II. Overview of Ultra-Low Voltage VCO-Based SD-FE Comparing RO Vs RxO

This section briefly reviews the VCO-based SD-FE operating at ultra-low supply voltage followed by comparison of the RO against the RxO.

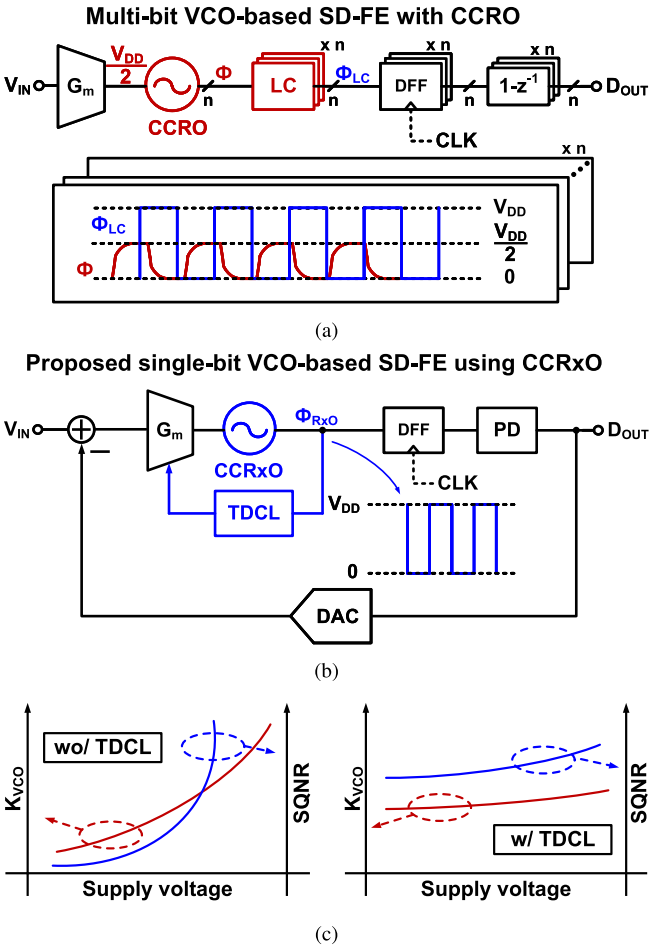

Fig. 2. (a) Multi-bit VCO-based SD-FE with CCRO, (b) proposed single-bit VCO-based SD-FE with CCRxO and TDCL, and (C) K_{VCO} related SQNR variation over supply without/with TDCL.

Fig. 2(a) shows the architecture of an open-loop n-bit VCO-based SD-FE [6]. The G_m stage and current-controlled ring oscillator (CCRO) together form a VCO that performs the V-F conversion and integration. The digital outputs are then generated by differentiating the two consecutive samples to realize a first-order noise shaping. The digital-intensive design reduces the system complexity by eliminating the headroom constraint in analog circuits while being highly area efficient. However, the open loop architecture has low SNDR limited by VCO linearity. The performance limitations in the open-loop architecture has been addressed by several circuit techniques in recent works, such as the use of: (i) negative feedback [27] (also adopted in this work), (ii) differential pulse code modulation [8] to improve VCO linearity, and (iii) phase and frequency detector (PFD) based phase quantizer to extend the dynamic range [7].

When operating under ultra-low supply, the multi-bit architecture tends to be more sensitive to delay cell mismatch, resulting in non-uniformly distributed quantization noise floor [25] and in-band spurs [28]. In addition, level converters (LC) [7] or sense amplifier flip-flop (SA-FF) [29] are required to recover the limited swing of the CCRO and avoid any false triggering of the sequential logic. However, their propagation delay highly depends on the input signal

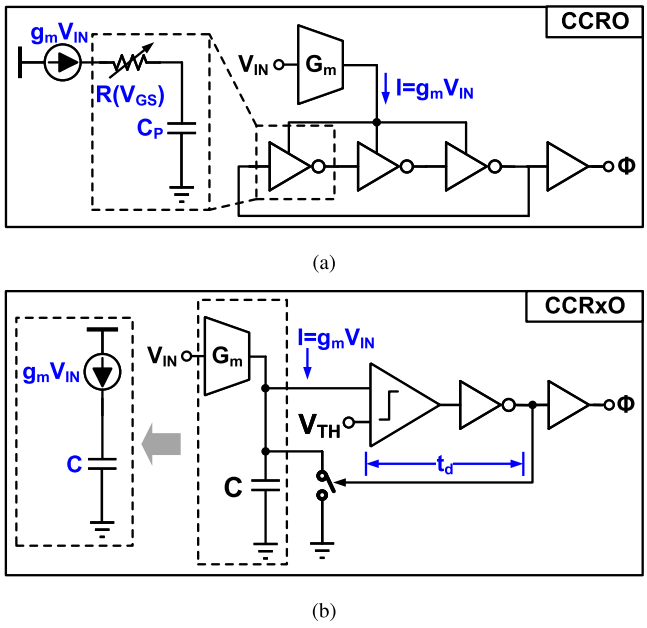

Fig. 3. G_m stage with (a) a three-stage CCRO, and (b) a CCRxO.

amplitude because of the G_m stage different biasing point. This induces signal-dependent excessive delay and short-circuit current, which could potentially cause large harmonic distortion. More importantly, as the output voltage of the energy harvesters are dependent on environment and use conditions, the VCO gain, K_{VCO}, varies accordingly. The quadratic relationship between the K_{VCO} and SQNR [6] can be described as:

$$SQNR = 9V_{in}^2\left(\frac{N}{2\pi}K_{VCO}\right)^2\frac{f_s}{f_B{}^3} \quad (1)$$

where V_{in} is the input signal amplitude and N represents the number of CCRO stages. The above equation yields a much severe variation in SQNR as shown in Fig. 2(c) (left).

In contrast to RO, RxO, often used as on-chip frequency reference [30], have an inherent single-phase output that can be adopted into a single-bit system. Moreover, the rail-to-rail swing eliminates the need for LC or the SA-FF, where a standard cell DFF can simply be used as the frequency sampler. This avoids the signal dependent delay and short-circuit current. Lastly, RxO tends to have a more linear tuning characteristic than RO (explained further) and hence a higher SNDR can be achieved. Fig. 2(b) illustrates the proposed single-bit VCO-based SD-FE, where a current-controlled relaxation oscillator (CCRxO) replaces the CCRO. Besides, the TDCL corrects the K_{VCO} variation with respect to supply by adjusting its center frequency such that the SQNR stays constant over a wide range as shown in Fig. 2(c) (right).

Fig. 3(a) shows a G_m stage driving a three-stage CCRO whose oscillation frequency is determined by the inverter propagation delay. Assuming an ideal G_m stage where the V-I relationship is linear, the main source of nonlinearity comes from the on-resistance and parasitic capacitor of the transistor in the inverter, which highly relies on the V_{GS} across it during the transition. The V_{GS} could be quite small considering the voltage drop across the G_m stage and even smaller under the ultra-low supply which pushes the devices into sub-threshold region with an exponential V-I curve. In the CCRxO shown in Fig. 3(b), the G_m stage directly charges the capacitor, C, can operate more linear than the CCRO. The oscillation frequency of the CCRxO can be written as,

$$f_{CCRxO} = \left(\frac{CV_{TH}}{g_m V_{IN}} + t_d\right)^{-1} \quad (2)$$

where t_d is the propagation delay of the comparator and the inverter, and V_{TH} is the reference voltage. If t_d is designed to be much smaller than the first term, the V-F characteristic of the G_m stage and CCRxO can be made linear to the first order, yielding the K_{VCO} to be,

$$K_{VCO} = \frac{g_m}{CV_{TH}} \quad (3)$$

Fig. 4 compares the simulated frequency deviation from the ideal V-F characteristic between the CCRO and CCRxO, where the two VCOs are designed with the same center frequency, f_c, setting to be 64 kHz and 128 kHz respectively. In order to only capture the linearity of the CCRO and CCRxO, ideal G_m stage with the same transconductance is used for the two simulations. The comparator in the CCRxO is implemented with an inverter-based stage to minimize the propagation delay which will be discussed in Section IV. It can be observed from Fig. 4 that the CCRxO is more linear than the CCRO for both the cases with different f_c settings. Table I briefly summarizes the pros and cons of the CCRO and the CCRxO.

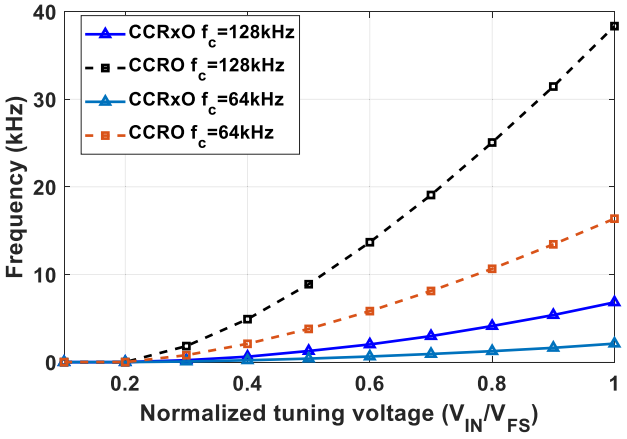

Fig. 4. Comparison between the simulated frequency deviation from the ideal V-F curve of a G_m stage with a three-stage CCRO and a CCRxO under different frequency settings.

TABLE I
COMPARISON BETWEEN THE CCRO AND CCRXO

	CCRO	CCRxO
Linearity	-	+
Delay cell mismatch	Yes	No
Require LC or SA-based digital interface	Yes	No
Single-bit system	Yes	Yes
Multi-bit system	Yes	No

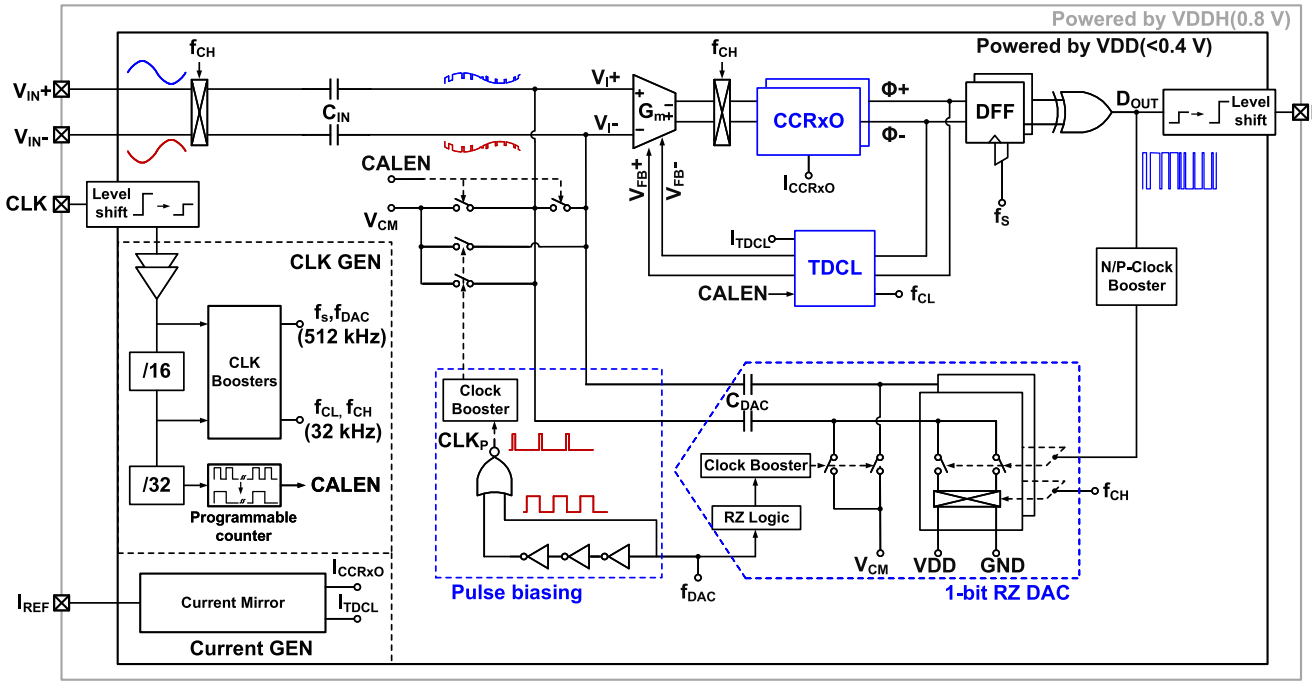

Fig. 5. Simplified block-level diagram of the proposed VCO-based SD-FE.

III. System Architecture of the Proposed VCO-Based SD-FE

The simplified circuit diagram of the proposed SD-FE is shown in Fig. 5. The input differential signals, $V_{IN}+$ and V_{IN}-, are capacitively-coupled to the G_m stage, where the V-I conversion is performed. The G_m stage is chopped to reduce the impact of the input-referred DC offset and flicker noise. The following CCRxO converts the current into phase information, $\Phi+$ and Φ-, which are then sampled by the DFF. A XOR-based phase detector (PD) further encodes the phase difference of the differential path into pulse-width modulated digital output, D_{OUT}. Note that D_{OUT} is a single-bit code because of the single-phase output of the CCRxO. In this case, a 1-bit return-to-zero digital-to-analog converter (RZDAC) is implemented to convert the digital output back to analog to realize a first-order $\Delta\Sigma$ loop, where the DAC references are chopped for proper feedback. The signal swing at the virtual ground, V_I+ and V_I-, is well-suppressed by the loop gain which prevents the VCO from entering the non-linear region and improves linearity [31]. The clock signals and D_{OUT} are boosted to 2X VDD to sufficiently turn on the switches under the deep sub-threshold supply (discussed in the next section). The sampling frequency of the SD-FE, f_s, is set to 512 kHz with an oversampling ratio (OSR) of 256, whereas the chopping frequency, f_{CH} is selected to be 32 kHz. The TDCL corrects the K_{VCO} drift due to supply variation by comparing the output phases with a reference, f_{CL}, generated on-chip. The error is then fed back to the G_m stage.

With the TDCL, the circuit operation can be divided into two paths which corresponds to two modes: calibration mode (CALEN=1), and data conversion mode (CALEN=0) respectively. During the calibration mode, the data conversion is disabled. The supply change is sensed by the VCO and converted into phase difference, then captured and fed back to the input G_m stage. The circuits enter the data conversion mode after the calibration completes. The TDCL will be turned ON periodically to monitor the real-time supply drift across time and refresh the correction information as discussed in Section IV. As the circuit is switched between two modes, a fast transition in between is desired to avoid unexpected settling errors during the transition, where the virtual ground nodes, V_{I+} and V_{I-}, play a central role. In contrast to the previous works biasing the input G_m stage through pseudo resistors which is unfriendly with mode switching, we propose a pulse biasing scheme by shorting the two nodes through a pair of pulse-driven switches to V_{CM} only during the RZ phase. This will be discussed in detail in Section IV.

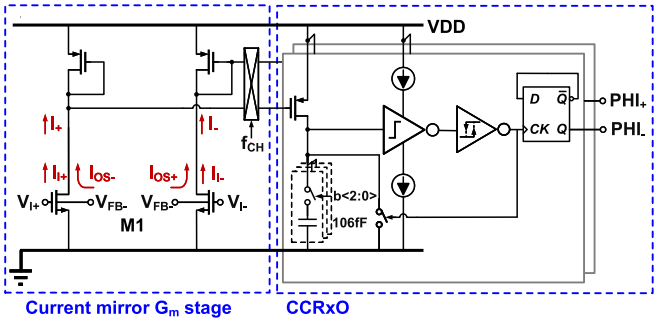

Fig. 6. Proposed G_m stage with the CCRxO.

IV. Circuit Implementation of the Proposed SD-FE

This section describes the circuit implementation of the G_m stage, the CCRxO, and the clock boosting circuits for ultra-low voltage followed by the design of the proposed TDCL and its sub-circuits to calibrate the K_{VCO} variation across supply.

Lastly, the pulse biasing scheme is presented that enables fast switching between calibration and data conversion modes.

A. G_m Stage and CCRxO

Fig. 6 shows the simplified circuit diagram of the proposed G_{m} stage and CCRxO. The G_{m} stage is implemented using the pseudo-differential current mirror architecture. The input differential pair M1 in the current mirror G_{m} stage biased to V_{CM}, defines the DC bias current, $I_{\mathrm{I}}+$ and I_{I}-. The feedback voltage from the TDCL is connected to the bulk of the input differential pair, modulating the threshold voltage of the input devices and providing additional offset current, $I_{\mathrm{OS}+}$ and $I_{\mathrm{OS}-}$. The sum of the offset current and the input current defines the final calibrated current that is mirrored into the CCRxO. The K_{VCO} in this case can be written as,

$$K_{\mathrm{VCO}} = \frac{g_{\mathrm{m}}}{CV_{\mathrm{TH}}} = \frac{I_{\mathrm{d}}}{nV_{\mathrm{T}}} \cdot \frac{1}{CV_{\mathrm{TH}}} \tag{4}$$

where the first term is the transconductance in subthreshold, n is the subthreshold slope factor, V_{T} is the thermal voltage, and I_{d} is the final calibrated current, calculated to be $I+I_{\mathrm{OS}}$. Therefore, by varying the biasing current I_{d}, the K_{VCO} can be adjusted, whereas the K_{VCO} is fixed for a given oscillating frequency. In the CCRxO, a pulse is generated when the comparator detects the instant the voltage accumulated on the capacitor crosses the inverter threshold. Hysteresis is embedded by the schmitt trigger to improve the noise immunity, after which the DFF converts the pulse into square wave. The comparator is implemented with inverter-based structure whose switching threshold is designed to be at VDD/2. The inverter-based comparator, realized with medium-V_{TH} transistors, ensures minimum propagation delay and its digital implementation makes it well-suited for ultra-low supply operation. Current-starved logic is adapted in the comparator, implemented with standard-V_{TH} transistors, to limit both the peak and the leakage currents. The comparator biasing current is designed to be 40 nA ensuring the propagation delay is small enough to not affect the oscillation frequency. The CCRxO has 3-bit coarse tuning capacitor allowing operation over a wider supply range.

B. Clock Boosting Circuits

Switches are extensively used in the DAC and choppers but are hard to turn ON at ultra-low supply. The weak turn ON raises the noise floor and further induces large signal dependent delay in the DAC causing significant distortion. Though increasing transistor size can reduce the ON resistance, it adds more node parasitics and suffers from charge injection. Therefore, clock booster circuits [32] are adopted in the design to sufficiently turn ON the switches while the transistor sizes can be maintained small. There are two sets of clock boosters chosen in the design. One set is for the choppers around the G_{m} stage in the forward path and another set is for the switches in the feedback DAC. NMOS switches with the N-type clock boosters as shown in Fig. 7(a) are chosen in the chopper around the G_{m} stage as it only needs to pass signals around V_{CM}. The N-type clock booster

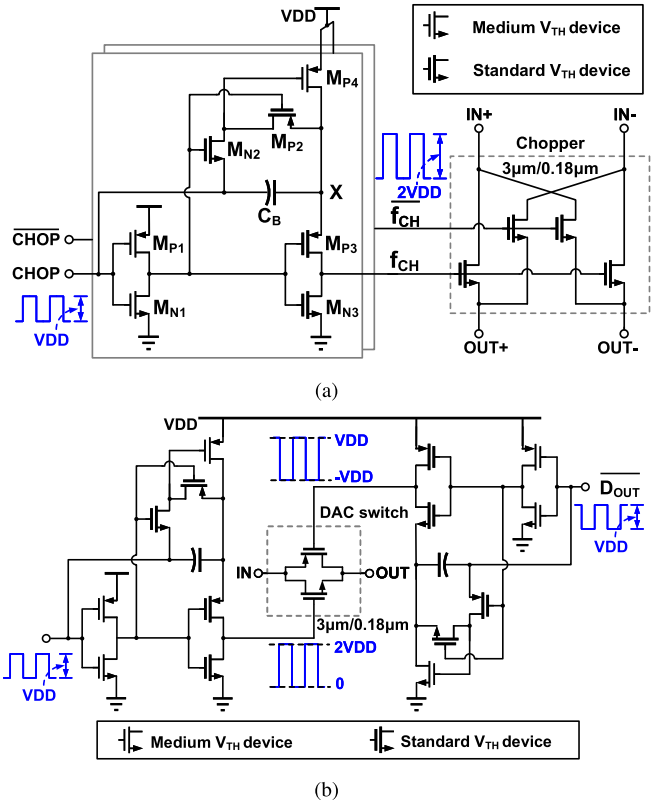

Fig. 7. (a) N-type clock boosters used in the chopper near the G_{m} stage, and (b) combined N/P-type clock boosters used for the switches in the DAC.

ideally boosts up the clock swing from 0-VDD up to 0-2VDD assuming there is no charge sharing loss. The effective V_{GS} of the switches is approximately 2VDD-V_{CM}. In contrast to the chopper switches around the G_{m} stage, the switches and choppers in the DAC are implemented with the transmission gate allowing both VDD and GND to pass through. N- and P- type clock boosters are combined to level shift the clock swing to 0-2(VDD) and −VDD-VDD, respectively as shown in Fig. 7(b). Therefore, the effective V_{GS} across the switch is always 2VDD.

The operation and design optimization of the clock booster for the NMOS switch are explained as follow. As shown in Fig. 7(a), when the input is low, M_{N3} is turned on and the output is low. At the same time, M_{P4} is turned on as M_{N2} pulls its gate to low. To make sure the top plate of the capacitor, C_{B}, is fully charged to VDD, medium V_{TH} device is selected for M_{P4} which offers a much lower on resistance compared to the standard V_{TH} device. Secondly, after the input of the clock booster switches to high, the top plate of C_{B} goes up to 2VDD as the charge held on C_{B} cannot change immediately. To maintain a high conversion efficiency, the charge stored on C_{B} shall not leak. There're two potential paths the charges may leak, one is through M_{P4} to VDD and the other is through M_{P3} and M_{N3} to ground. The gate of M_{P4} is connected to 2VDD during this phase ensuring it stays in deep cut off region where charge leakage is less likely to happen. On the other hand, if the propagation delay of the first inverter (consisting of M_{N1} and M_{P1}) is large, M_{P3} and M_{N3} may be turned on simultaneously leading to substantial charge loss to ground.

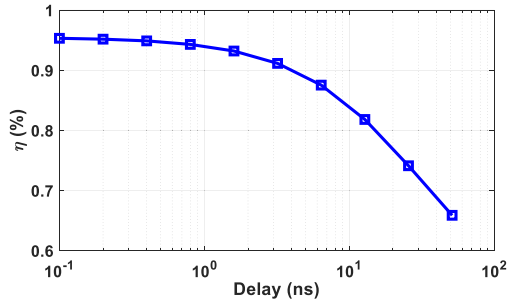

Fig. 8. Impact of the delay of the first inverter on the voltage conversion efficiency.

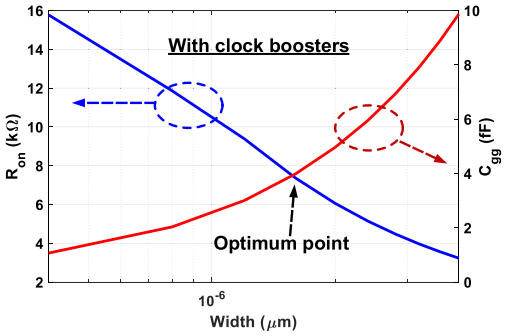

Fig. 9. Optimum size of the NMOS switch with clock boosters.

To quantify this delay dependency, Fig. 8 plots the simulated conversion efficiency against the propagation delay of the first inverter, where the efficiency is defined as,

$$\eta = \left(\frac{V_{\rm bst}}{2VDD}\right) \times 100\% \tag{5}$$

where $V_{\rm bst}$ is the actual boosted voltage. The efficiency drops dramatically if the delay exceeds 1 ns which can be common with standard $V_{\rm TH}$ devices under ultra-low supply. Therefore, medium $V_{\rm TH}$ devices are adopted for the first inverter to reduce its propagation delay, making sure $M_{\rm N3}$ can be turned off immediately after the input switches. Thirdly, the charge sharing between $C_{\rm B}$ and the parasitics at node X can further degrade the efficiency. To alleviate its effect, the value of $C_{\rm B}$ is selected to be 4 pF to help resist the parasitic impact. Additionally, the top plate of $C_{\rm B}$ is connected to node X instead of the bottom plate. Transistors connected to this node are sized small to further reduce the parasitics. As a result, the simulated efficiency of the clock booster is more than 98%, which can be traded off with other parameters such as power area and speed to get the optimum performance.

The optimum point of the size of the switch with the clock boosters is found by simulating both the ON resistance and parasitic capacitors of the switch as shown in Fig. 9. A NMOS transistor with minimum length is selected while its width is swept to find the optimum point. Fig. 9 shows the simulated ON resistance, $R_{\rm on}$, and the gate parasitic capacitance, $C_{\rm gg}$, with the clock boosters. The optimum width of the transistor from the simulation is 3.2 μm (two fingers), where the $R_{\rm on}$ and the $C_{\rm gg}$ are 7.3 kΩ and 4 fF, respectively. The same process is followed when designing the transmission gate where the optimum size of NMOS and PMOS transistors are selected to be both 3 μm/0.18 μm with a simulated $R_{\rm on}$ of approximately 6 kΩ.

C. TDCL Architecture

The simplified block-level diagram of the TDCL in the calibration mode (CALEN= 1) and data conversion mode (CALEN= 0) is illustrated in Fig. 10. Note that the necessary clock boosters have been omitted for simplicity. The TDCL consists of a frequency divider, a PFD, a low-leakage charge pump (LL-CP), and a loop filter (LF) with a built-in sample and hold (S/H). At the beginning, the circuit enters the calibration mode by setting the enable signal, CALEN, to one. The differential inputs of the $G_{\rm m}$ stage are shorted with the choppers bypassed. The VCO (including the $G_{\rm m}$ stage and CCRxO) senses the supply variation and then converts this information into frequency domain. The pseudo differential CCRxO outputs are divided by two and compared with the reference, $f_{\rm CL}$ (= 32 kHz), derived from the sampling clock, $f_{\rm s}$. An additional delay is introduced after $f_{\rm CL}$ to match the delay created by the frequency divider. The PFD extracts the phase lead and lag information between the divided CCRxO output and $f_{\rm CL}$. The LL-CP integrates the phase error and converts it back to voltage domain. The converted voltage is then fed back to the $G_{\rm m}$ stage in the VCO through the auxiliary $G_{\rm m}$ described in Section IV.A. As a result, the auxiliary $G_{\rm m}$ injects the offset current into the CCRxO and corrects any shift in center frequency back to twice of $f_{\rm CL}$. After the calibration is done, CALEN is set to zero and the TDCL is turned OFF with the correction signal sampled on the capacitor, C_2. Rest of the circuits are simultaneously enabled to enter the data conversion mode. The TDCL is duty cycled in an auto-zeroed manner where it will be re-connected back after a certain amount of time to compensate the charge leakage through the switch and refresh the voltage on C_2 (refer next sub-section). Note that the TDCL is also able to correct any mismatch inside the $G_{\rm m}$ stage and the CCRxO which yields a low input-referred offset.

Fig. 11 illustrates the simulated $K_{\rm VCO}$ variation across a wide supply range when the TDCL is enabled and disabled. With a center frequency of 64 kHz, the $K_{\rm VCO}$ remains almost constant with a $\Delta K_{\rm VCO}$ of approximately 0.1 MHz/V over 0.2 V supply variation when the TDCL is ON. The simulated $\Delta K_{\rm VCO}$ is more than 40X lower than the case when the TDCL is OFF.

D. Design of the LL-CP

The charge leakage from C_2 during the data conversion mode needs to be small enough to minimize any frequency change in the VCO. The most critical leakage path is from the sampling switch and CP to the GND or VDD. Therefore, reducing the leakage of the switch and CP during their OFF state plays a central role in lowering the leakage-dependent VCO frequency variation.

Fig. 12 illustrates the transistor level schematic of the LL-CP combined with a low leakage sampling switch. The UP/DN control switches in the CP are connected between the current mirrors and the rails to maintain a low ON-resistance

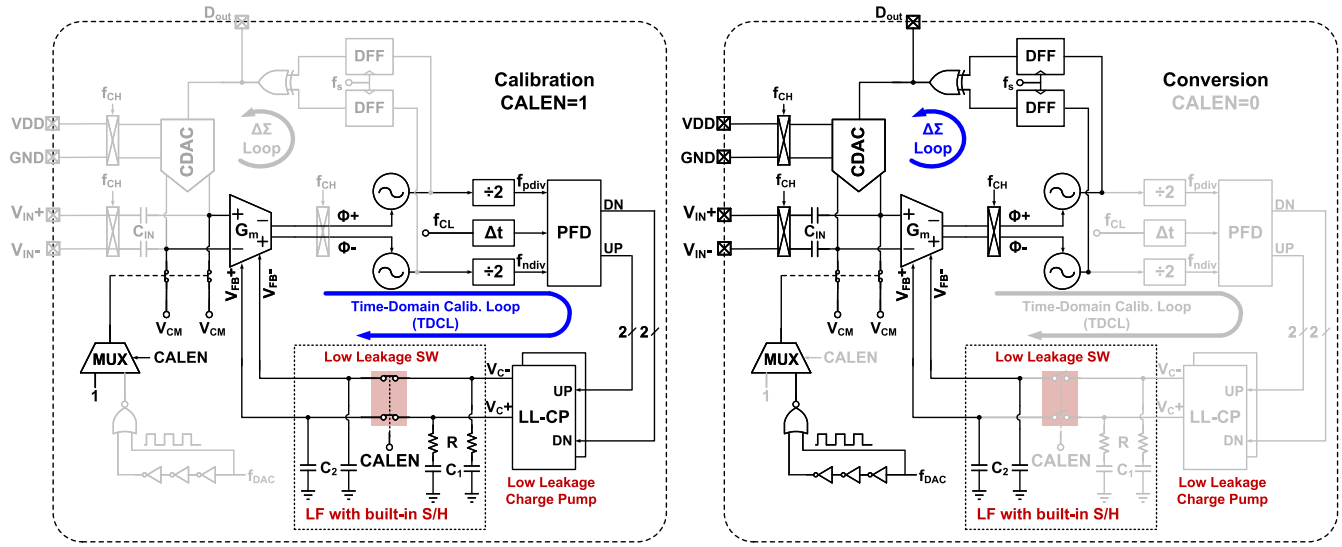

Fig. 10. Simplified block-level diagram of the proposed TDCL in different phases.

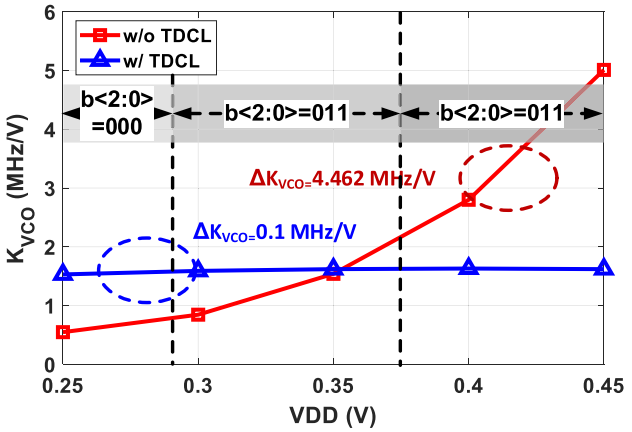

Fig. 11. Simulated ΔK_{VCO} over supply variation with and without the TDCL.

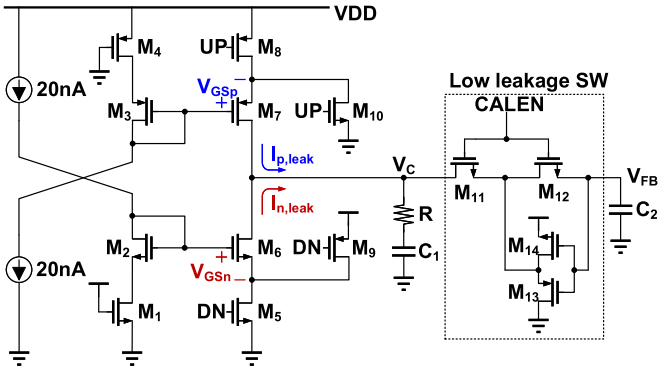

Fig. 12. LL-CP with the low leakage sampling switch.

at ultra-low supply voltage. An additional pair of NMOS and PMOS switches, M_9 and M_{10}, are placed in parallel with the current mirror to pull the source nodes of the current mirrors to VDD and GND respectively. This ensures a low V_{GS} across the current mirror and reduces the off-state leakage.

The sampling switch employs two NMOS transistors, M_{11} and M_{12}, connected in series to increase its effective OFF resistance. The source follower-based feedback [32] consisting of a leakage-based biasing transistor, M_{14} and PMOS source follower, M_{13}, ensures that the switch internal node tracks the sampled voltage on C_2 to further reduce the switch leakage. Therefore, the charge leakage from C_2 can be significantly reduced to maintain a constant voltage hold on C_2 with a minimum amount of voltage droop during its off time. The resistor, R, in the LF is designed to be 1 MΩ. The capacitors, C_1 and C_2, are selected to be 108 pF and 10.8 pF respectively, which reuse the same area with the on-chip decoupling capacitor to save the overall area.

Simulation results in Fig. 13 demonstrates the advantages of the proposed LL-CP combined with the low-leakage switch (LL-SW), where both the leakage of the CP and the voltage droop across C_2 are simulated across corners. Substantial leakage and voltage droop reduction can be observed across five process corners, among which the worst case leakage and voltage droop happened at fast-fast (ff) corner are 146 pA and 12.1 mV/s, respectively.

The output signal of the LF perturbates due to the noise that is contributed by the CP and the resistor, R, which will then be converted into current by the G_m stage. This noise must be taken into consideration as it can be transferred to the output and therefore raise up the noise floor. Fortunately, the output signal, V_{FB}, is sampled on the capacitor C_2 after the calibration is done where the noise can be considered as kT/C noise similar to a sample-and-hold system. Once the signal is sampled on C_2, the voltage held on the capacitor is frozen to a fixed value as shown in Fig. 14 where it can be considered as a small DC offset. Hence, similar to the kT/C noise cancellation in [33], the thermal noise is first converted into DC offset and is then upmodulated to the chopping frequency by the second chopper at the output of the G_m stage after amplified by the g_{mb}. As a result, the noise contributed by the TDCL acts as a DC offset after sampling which is eventually handled by the output chopper.

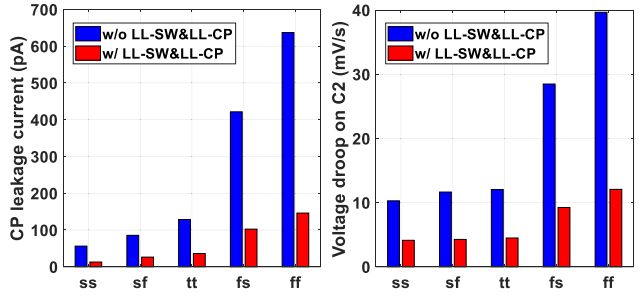

Fig. 13. Simulation results of the CP leakage current and the voltage droop on the sampling capacitor C_2 across corners.

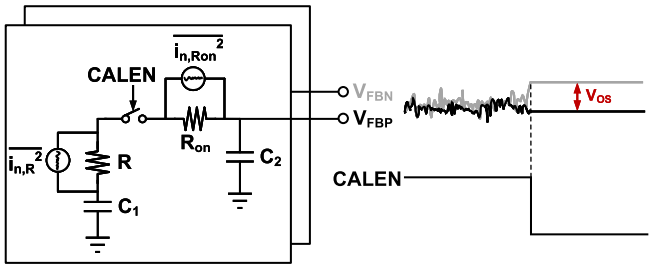

Fig. 14. Noise contributed by the LF that is sampled on C_2 and its time domain waveform.

E. DAC Design With the Pulse Biasing

The DAC converts the digital output to analog and feeds back the signal to the input. Fig. 15 illustrates the single-ended circuit implementation of the RZDAC (chosen to mitigate inter-symbol interference errors) with its timing diagram, where the clock boosters and transistor level schematic of the switches and choppers are not shown for simplicity. As mentioned in Section IV. B., the input chopper is implemented with NMOS switches, while the switches in the DAC are implemented with transmission gate. The RZ output data, D_{RZ} and Db_{RZ}, are generated from the non-return-to-zero (NRZ) output, D_{OUT}, driving the switches in the DAC. The DAC works as a floating battery, where the transition on one of the terminals of the capacitor in the DAC couples to the other terminal. The output of the DAC can be expressed as,

$$V_{\mathrm{I}} = \left(\frac{C_{\mathrm{IN}}}{C_{\mathrm{IN}} + C_{\mathrm{DAC}}}\right) V_{\mathrm{IN}} - \left(\frac{C_{\mathrm{DAC}}}{C_{\mathrm{IN}} + C_{\mathrm{DAC}}}\right) V_{\mathrm{DAC}} \quad (6)$$

where V_{DAC} is the reference voltage of the DAC, which is effectively VDD/2 (D_{RZ}=1), -VDD/2 (Db_{RZ}=1), and 0 V (CLK_{RZ}=1). The chopper in the DAC simply changes the polarity of the feedback signal by switching the references between VDD and GND, matching the polarity of the input signal after the input chopper for proper feedback.

A closer look at the virtual ground nodes at the input of G_{m} stages indicates that the RZDAC feedback sees a floating node that is undefined during the data conversion mode. Prior works [6]–[8] have used pseudo resistor to define the common-mode biasing voltage while maintaining a large resistance without significantly loading the DAC. However, the large RC time constant formed by the input capacitor, C_{IN}, and the pseudo resistor leads to a long settling time that can go upto tens or hundreds of milli-seconds, invalidating the output digital codes. To accelerate this process, a pulse biasing scheme is implemented as shown in Fig. 15, where a pulse signal is generated from the RZ clock, CLK_{RZ}, through a pulse generator (PG). Additional common-mode current is injected into the virtual ground nodes through a switch which defines the common-mode voltage. The amount of current that is injected into the node can be dynamically adjusted based on the common-mode voltage, which substantially speeds up the settling process. Additionally, in the steady-state, compare to the pseudo resistor whose resistance varies non-linearly with the voltage across it, a better linearity can be achieved as the effective resistance of the pulse biasing scheme simply depends on the duty cycle of the pulsed clock and the switch on-resistance.

V. Measurement Results

The proposed VCO-based SD-FE was fabricated in 180 nm CMOS with a total area of 0.9 mm^2 and an active area of 0.12 mm^2 with the die micrograph shown in Fig. 16. The active areas of the SD-FE, the TDCL, and the CLK GEN are 0.063 mm^2, 0.0245 mm^2, and 0.03mm^2, respectively, where nearly half of the active area in the SD-FE is consumed by the clock booster circuits.

The chip is measured with the following setup unless otherwise noted. The sampling frequency and chopping frequency are set to be 512 kHz and 32 kHz, respectively, whereas a 350 mV supply is provided. The duty cycle ratio of the TDCL is programmed through the on-chip counter to be approximately 0.024 %. The differential input signal is generated from the Keysight 33500B Signal Generator with the amplitude attenuated to the proper level. The digital output is post-processed using MATLAB. A −3.88 dBFS peak-to-peak differential input signal at 100Hz is applied at the input with every block activated. Fig. 17 shows the measured SD-FE output spectrum (2^{21} FFT points with hanning window). Benefited from the feedback architecture and CCRxO, the harmonic distortion can be maintained relatively small with visible HD2 and HD3 components, where the HD3 dominates the overall distortion because of the pseudo differential architecture. The measured SNDR and spurious-free dynamic range (SFDR) within 1 kHz bandwidth are 61 dB and 79 dB respectively. The chopper pushes the flicker noise corner to below 1 Hz while upmodulating the residue offset to the chopping frequency after the TDCL operation.

Fig. 18 shows the measured DR plot of the SD-FE. By sweeping the amplitude of the input sinusoidal signal (100 Hz), the measured peak SNDR is 63.2 dB at V_{in}=−1.94 dBFS. The measured DR is 66 dB, yielding an input-referred RMS noise of 4.43 μV_{RMS} and an effective noise power spectral density of approximately 140.1 nV/$\sqrt{\mathrm{Hz}}$. Fig. 19 illustrates the measured SNDR across the targeted frequency range. An input signal with full-scale amplitude is applied with its frequency swept from 1 Hz to 1 kHz. It can be observed in Fig. 19 that the SNDR is almost constant with a variation of less than 0.5 dB over the targeted frequency.

In order to validate the effectiveness of the TDCL, the supply sensitivity of the SD-FE is measured as shown in Fig. 20. First, the TDCL is configured off while the supply voltage is swept from 0.3 V to 0.5 V. A smaller input amplitude of −7.96 dBFS is selected to avoid the large K_{VCO} variation

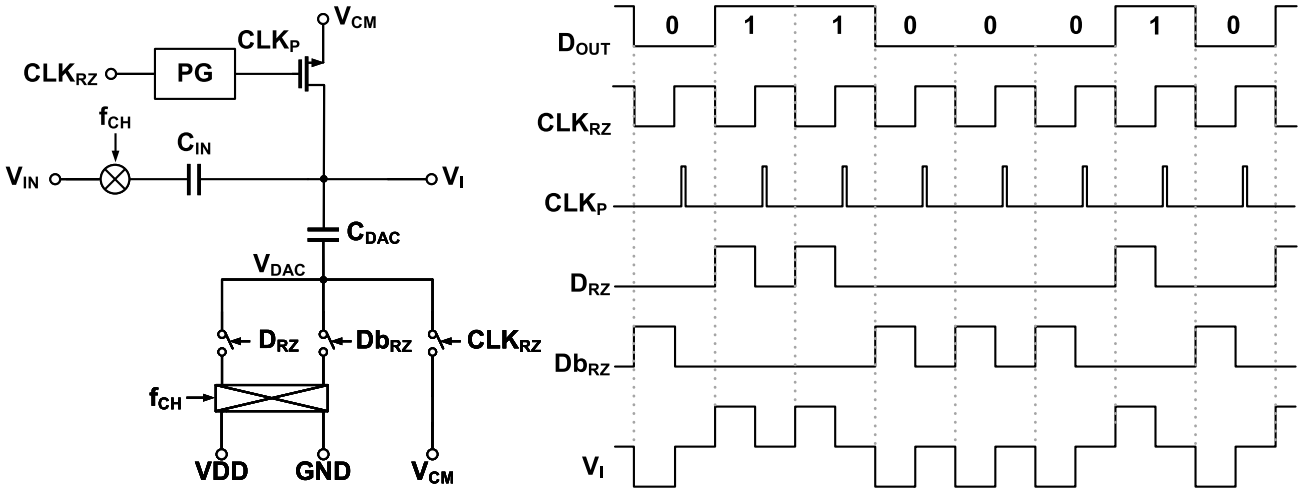

Fig. 15. Single-ended circuit implementation of the DAC with the pulse biasing scheme and its timing diagram.

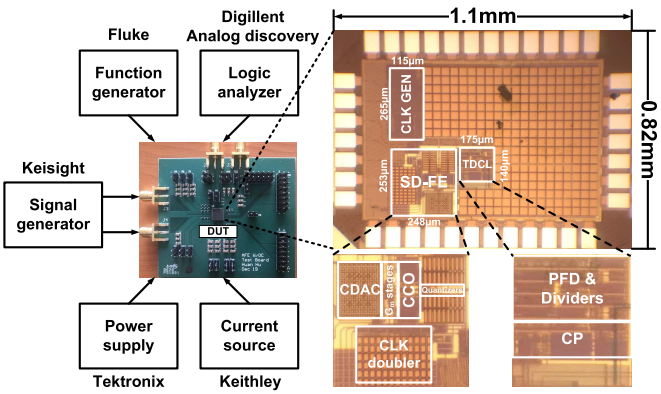

Fig. 16. Chip die micrograph and the measurement setup.

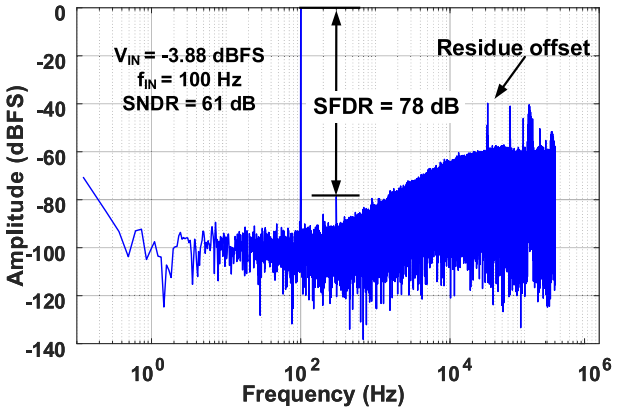

Fig. 17. Measured output spectrum of the proposed SD-FE.

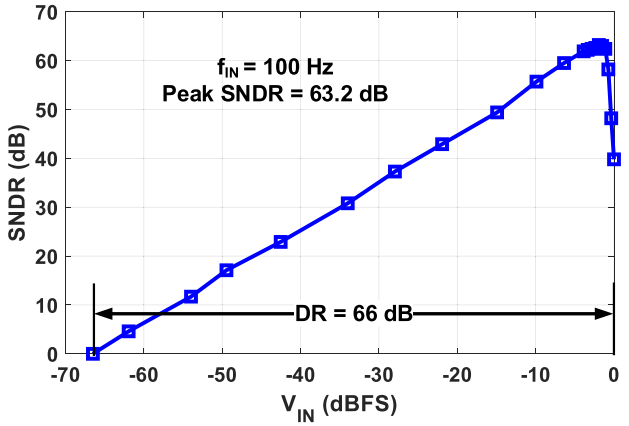

Fig. 18. Measured SNDR vs. input amplitude.

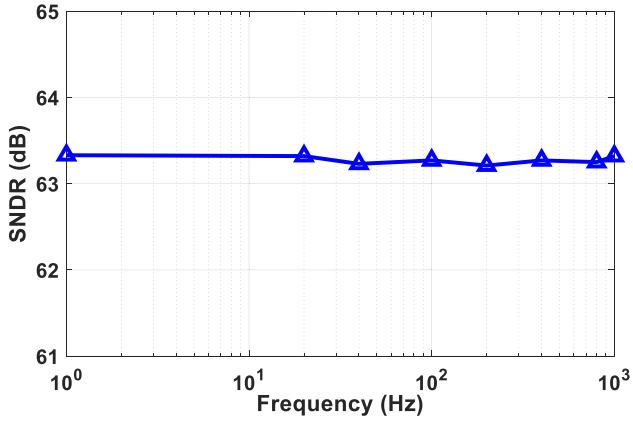

Fig. 19. Measured SNDR vs. frequency.

destabilize the $\Delta\Sigma$ modulator. As can be observed from Fig. 20, the measured SNDR varies significantly when the TDCL is off. Notably, the SNDR of the last two points is even smaller compared to the first three points, which is mainly because of the large K_{VCO} saturating the phase quantizer. Once the TDCL is turned on, the measured SNDR variation can be significantly reduced, yielding an overall ΔSNDR of only 1.7 dB over the entire range which is 9.3 dB smaller than the case when the TDCL is disabled.

Although chopper upmodulates the major DC offset from the input G_{m} stages, the mismatch of the pseudo differential CCRxO and the chopper switches create residue offset that cannot be handled by the chopper. The input DC offset performance can be further improved by the TDCL and is measured with the following procedure. First, a 2 mV DC input is applied to the SD-FE with its output spectrum recorded as a reference. Then the differential inputs of the SD-FE are

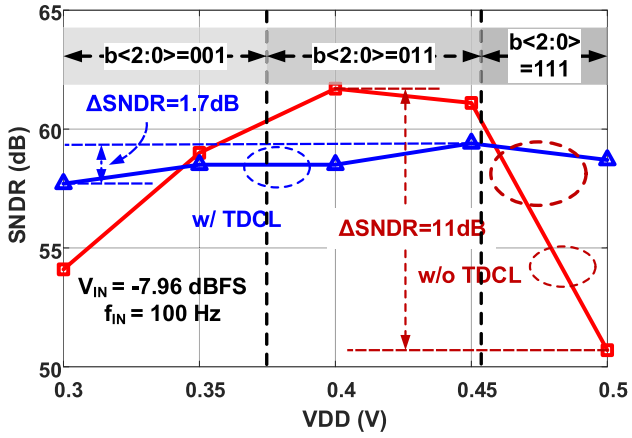

Fig. 20. Measured SNDR variation vs. VDD with and without the TDCL.

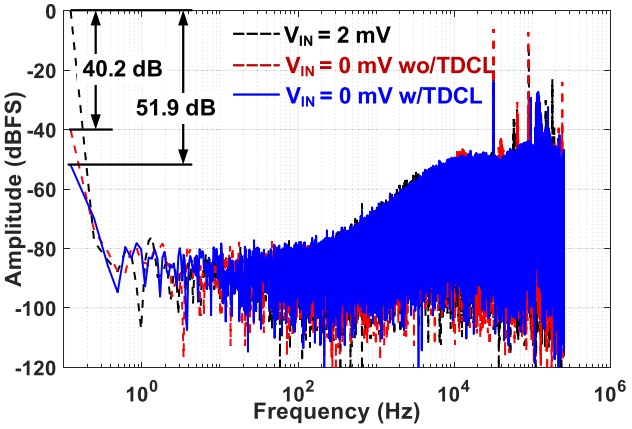

Fig. 21. Measured input-referred DC offset with and without the TDCL.

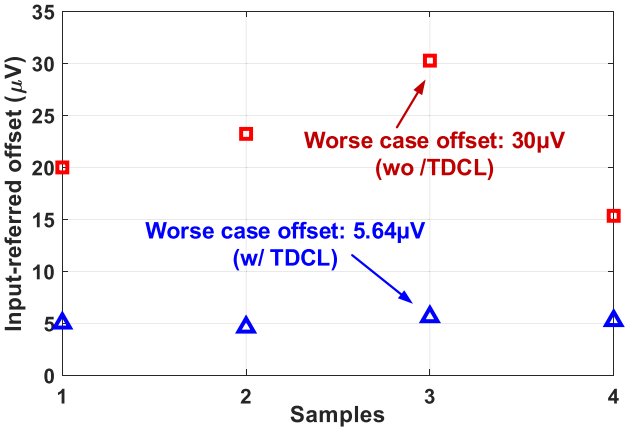

Fig. 22. Measured die-to-die vairiation of the input-referred offset with and without the TDCL.

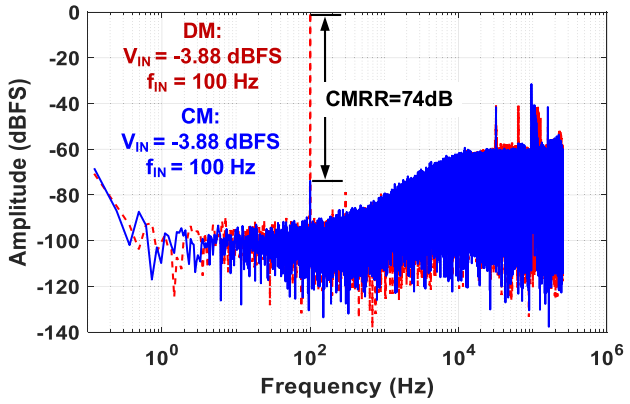

Fig. 23. Measured output spectrum with DM and CM input signal.

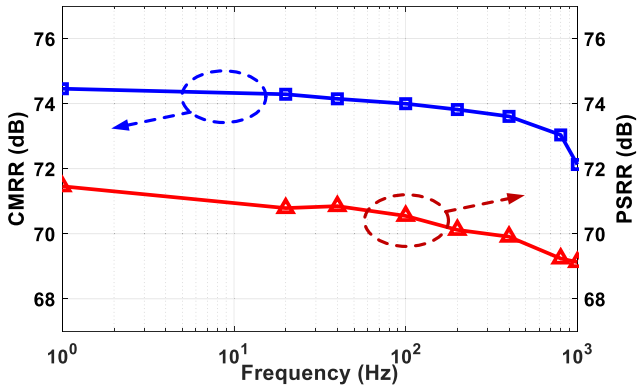

Fig. 24. Measured CMRR and PSRR vs. frequency.

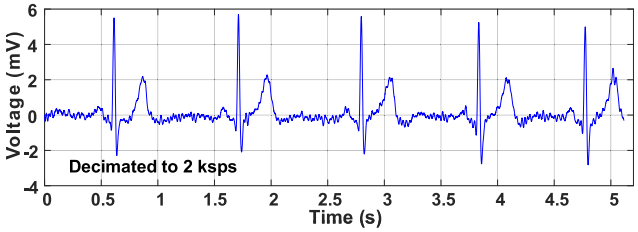

Fig. 25. Measured ECG signal decimated to 2 ksps.

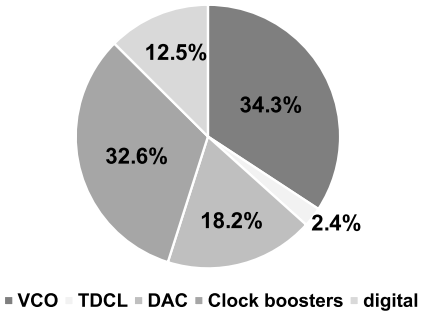

Fig. 26. Power breakdown diagram.

shorted to simply measure the offset, where the measurement is done with the TDCL disabled and enabled, respectively. Fig. 21 demonstrates the measurement results for the three cases. An 11.7 dB improvement can be observed when the TDCL is turned ON, indicating an input referred DC offset of 5.08 μV. The die-to-die variation of the input-referred offset is also validated by measuring 4 different samples. Fig. 22 shows the measured results. When the TDCL is disabled, the worst case input-referred offset is measured to be approximately 30 μV, whereas a worst case input-referred offset of 5.64 μV is observed after enabling the TDCL.

The common-mode rejection ratio (CMRR) is measured by applying both a differential-mode (DM) and common-mode (CM) input signal with -3.88 dBFS amplitude at 100 Hz. Fig. 23 shows the measured output FFT for the two cases, where a CMRR of 74 dB can be observed. Measurement results in Fig. 24 show a CMRR of >72 dB and a

TABLE II

PERFORMANCE SUMMARY AND COMPARISON OF THE PROPOSED ULTRA-LOW VOLTAGE SD-FE WITH STATE-OF-THE-ART

	This work	[34] SSCL'18	[35] JSSC'18	[23] JSSC'15	[22] JSSC'12	[19] JSSC'18	[16] JSSC'19	[25] SSCL'18	[11] JSSC'12
Type	Voltage sensor						ADC		
Approach	VCO	VCO	VCO	Gm-C+VCO	OTA+VCO	Passive	OTA	VCO	OTA
Tech. (nm)	180	65	65	130	65	65	130	28	130
VDD (V)	0.35	0.6	0.5	0.5	0.5	0.3	0.3	0.2	0.25
Power (μW)	0.22	3.2	1.275	2.3	5.04	0.18	79.3	7	7.5
f_s (MHz)	0.512	0.001	-*	0.001	0.02	0.256	2.56	30	1.4
BW (kHz)	1	0.5	11	0.5	10	3	20	61	10
SFDR (dB)	78	62	60	52	58	-	83.4	71.2	70
SNDR (dB)	63.2	51	54	-	45	60	74.1	67.4	61
DR (dB)	66	-	-	-	-	65	76.5	-	64
IRN (μV_{RMS})	4.43	2.2	3.8	1.29	4.9	-	-	-	-
ΔSNDR (dB) (VDD range)	1.7 (0.3-0.5)	- -	- -	- -	- -	7 (0.3-0.5)	- -	6.04 (0.178-0.214)	3.2 (0.25-0.6)
$\Delta SNDR_{nom}$ (dB)**	0.030	-	-	-	-	0.105	-	0.336	0.023
CMRR (dB)	72	77	60	88	75	-	-	-	-
PSRR (dB)	69	65	-	67	64	-	-	-	-
NEF/PEF	4.27/6.39	8.7/45.4	2.2/2.4	4.76/11.3	5.99/17.9	-	-	-	-
FoM_s (dB)	159.8	132.9	153.4	-	151.2	162.2	158	166.8	152.2
Area (mm^2)	0.12	0.01	0.006	0.025	0.013	0.195	0.74	0.0032	0.0195

NEF=$V_{RMS}\sqrt{\frac{2\cdot I_{total}}{\pi\cdot 4kT\cdot BW}}$ $\mathrm{PEF} = \mathrm{P_{total}} \cdot \frac{2\cdot V_{rms}^2}{\pi\cdot 4kT\cdot V_T\cdot BW}$; $\mathrm{FoM_s} = \mathrm{SNDR} + 10\log(\mathrm{BW/Power})$;

*-Asynchronous design; **-Normalized to per 1% supply variation.

power supply rejection ratio (PSRR) of >69 dB respectively over the frequency of interest. Fig. 25 demonstrates the recorded ECG signal decimated to 2 kS/s with the proposed SD-FE.

The measured power consumption of the proposed VCO-based SD-FE is 0.22 μW under 0.35 V supply. The G_m stage with the CCRxOs, the TDCL, the DAC, the clocking boosting circuits, and the digital circuits consume 75.5 nW, 5.32 nW, 40.2 nW, 71.8 nW and 27.6 nW respectively illustrated in Fig. 26. Besides the G_m stage with the CCRxOs, a large fraction of power is consumed by the clock booster circuits as it is extensively used to boost the clock signals. Careful design optimization can be incorporated in the future work to reduce this part of the power consumption.

Table II compares the proposed work with the state-of-the-art ultra-low supply designs including both the ADC and VCO-based sensor interface. The single-bit CCRxO with TDCL achieves one of the highest SNDR and SFDR for sub-0.4V time-domain SD-FE architectures while ensuring a stable SNDR over a wide supply range of 200 mV compared to other works. This range can further be enhanced by tuning the CCRxO in future. Besides, it also achieves one of the best noise efficiency factor (NEF) and power efficiency factor (PEF) as compared to both voltage sensor and ADC based architectures making it a promising architecture to directly operate with an energy harvester.

VI. CONCLUSION

This work demonstrates an ultra-low supply single-bit VCO-based sensor interface. The CCRxO as the phase domain integrator is uniquely integrated in this design, which is demonstrated to be more friendly with ultra-low voltage design in terms of both better linearity and lower power consumption compared to CCRO. A TDCL is also proposed with a leakage-optimized CP to counter the SNDR variation with respect to supply, which can be potentially adapted in direct energy harvester powered system. Compared to the state-of-the-art ultra-low voltage designs, the SD-FE achieves the lowest SNDR variation, while achieving comparable NEF/PEF and FoM_s. Additionally, this work creates new oppotunity for designers to incorporate RxOsx into VCO-based sensor interfaces, instead of being constrained only to ROs. Investigating multi-bit systems relying on the relaxation oscillator could be an interesting future research direction.

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