Cascaded Complex ADCs With Adaptive Digital Calibration for I/Q Mismatch

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***Abstract*—A complex analog-to-digital converter (ADC) intended for digital intermediate frequency (IF) receiver applications digitizes analog signals at IFs with excellent power/bandwidth efficiency. However, it is vulnerable to mismatches between its in-phase and quadrature (I/Q) paths that can dramatically degrade its performance. The proposed solution mitigates I/Q mismatch effects using a complex sigma-delta ($\Sigma\Delta$) modulator cascaded with 9-bit pipeline converters in each of the I and Q paths. The quantization noise of the first stage complex modulator is eliminated using an adaptive scheme to calibrate finite-impulse response digital filters in the digital noise-cancellation logic block. Although low-pass $\Sigma\Delta$ cascade ADCs are widely used because of their inherent stability and high-order noise shaping, the complex bandpass cascade architecture introduced herein maintains these advantages and doubles the noise shaping bandwidth. Digital calibration also reduces the effects of analog circuit limitations such as finite operational amplifier gain, which enables high performance and low power consumption with high-speed deep-submicrometer CMOS technology. Behavioral simulations of the complex $\Sigma\Delta$/pipeline cascade bandpass ADC using the adaptive digital calibration algorithm predict a signal-to-noise ratio (SNR) of 78 dB over a 20-MHz signal bandwidth at a sampling rate of 160 MHz in the presence of a 1% I/Q mismatch.**

***Index Terms*—Bandpass analog-to-digital converter (ADC), data converter, complex ADC, digital calibration, digital intermediate frequency (IF) receiver, in-phase and quadrature (I/Q) mismatch, sigma-delta ($\Sigma\Delta$).**

I. Introduction

THE proliferation of wireless communication devices drives the demand for highly integrated digitally intensive multi-standard RF transceivers. One strong candidate for such applications is the digital intermediate frequency (IF) receiver or software defined radio (SDR), which digitizes the down-converted analog signals at IF, and then performs further down-conversion and channel-selection filtering digitally [1]–[3]. The trend towards a digitally intensive approach is strongly suggested by Moore's Law, which favors high-speed low-power digital signal processing (DSP) solutions, and eliminates the conventional analog IF-to-baseband down-conversion that is susceptible to dc offsets, flicker noise, second harmonic distortion, etc., [2], [4]. However, the digital-IF receiver also digitizes only partially filtered close-in interferers in addition to the desired signal, and thus requires a high-speed analog-to-digital converter (ADC) with high dynamic range and linearity [5], [6]. Wide-band sigma-delta ($\Sigma\Delta$) ADCs with low oversampling ratios (OSR) (e.g., 4–16) are receiving considerable attention for such applications because of their high performance and scaling-friendly nature [7]–[9].

A complex bandpass data converter is attractive compared to its pipeline and low-pass $\Sigma\Delta$ counterparts because it digitizes quadrature analog signals directly at IF frequencies [10], [11]. Moreover, unlike a real bandpass $\Sigma\Delta$ converter, the poles and zeros of its noise transfer function (NTF) are not symmetric at dc, but rather around the intermediate frequency $f_{\rm IF}$. Thus, it provides twice the noise shaping as a real bandpass $\Sigma\Delta$ converter of the same order. A tradeoff is that complex converters are vulnerable to mismatches between the in-phase (I) and quadrature (Q) paths. As a result, interference at the ADC inputs and quantization noise in the image band are folded into the signal band and degrade the signal-to-noise ratio (SNR). Several methods have been proposed to mitigate I/Q mismatch effects in complex converters.

1) A data-dependent dynamic-element matching (DEM) algorithm improves the image rejection ratio (IRR), but applies only to single-bit digital-to-analog converter (DAC) mismatches [12].
2) I/Q mismatch effects are reduced by placing one or more transmission zeros in the NTF in the image band [13]. This solution exhibits lower-order noise shaping in the signal band and requires greater hardware complexity.
3) An adaptive noise cancellation technique allows the signal to be separated from interference aliased from the image band [14]. However, the folding of quantization noise from the image band into the signal band persists.
4) A DEM scheme for multi-bit quadrature modulators reduces path mismatch effects such as the folding of interferers into the signal band, but it introduces a self-image [15].

The cascade $\Sigma\Delta$ modulator architecture is attractive because it enables high-resolution quantization for a low OSR [7], [9], [16]. Consider the cascade modulator of Fig. 1 in which the quantization noise of the first stage, $Q1(z)$, is extracted and re-quantized by the second stage. The outputs of the two stages, $Y1(z)$ and $Y2(z)$, are then input to the noise-cancellation logic (NCL) block and combined as

$$Y(z) = \mathrm{STF2}_D(z)Y1(z) - \mathrm{NTF1}_D(z)Y2(z) \qquad (1)$$

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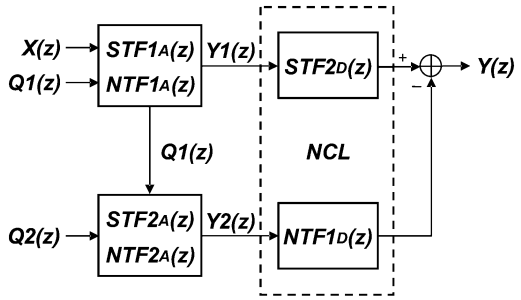

Fig. 1. Two-stage cascade modulator with digital NCL.

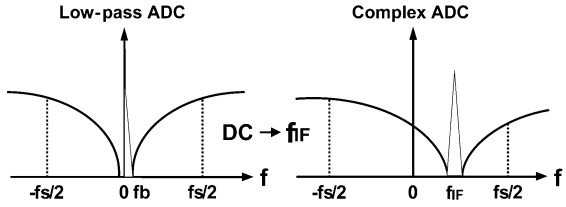

Fig. 2. Output spectra of low-pass and complex bandpass $\Sigma\Delta$ modulators.

where $\mathrm{STF2}_D(z)$ and $\mathrm{NTF1}_D(z)$ are digital filter approximations of the signal and noise transfer functions of the second and first stages, respectively. From Fig. 1

$$Y_1(z) = \mathrm{STF1}_A(z)X(z) + \mathrm{NTF1}_A(z)Q_1(z) \quad (2)$$
$$Y_2(z) = \mathrm{STF2}_A(z)Q_1(z) + \mathrm{NTF2}_A(z)Q_2(z) \quad (3)$$

where $\mathrm{STF1}_A(z)$ and $\mathrm{STF2}_A(z)$ are analog signal transfer functions, and $\mathrm{NTF1}_A(z)$ and $\mathrm{NTF2}_A(z)$ are analog noise transfer functions of the first and second stages, respectively. Combining (1)–(3) gives

$$\begin{aligned} Y(z) = {} & \mathrm{STF1}_A(z)\mathrm{STF2}_D(z)X(z) \\ & + [\mathrm{NTF1}_A(z)\mathrm{STF2}_D(z) \\ & - \mathrm{NTF1}_D(z)\mathrm{STF2}_A(z)]Q1(z) \\ & - \mathrm{NTF1}_D(z)\mathrm{NTF2}_A(z)Q2(z) \end{aligned} \quad (4)$$

With the NCL designed so that

$$\begin{aligned} \mathrm{STF2}_D(z) &= \mathrm{STF2}_A(z) \\ \mathrm{NTF1}_D(z) &= \mathrm{NTF1}_A(z) \end{aligned} \quad (5)$$

equation (4) simplifies to

$$\begin{aligned} Y(z) = {} & \mathrm{STF1}_A(z)\mathrm{STF2}_D(z)X(z) \\ & -\mathrm{NTF1}_D(z)\mathrm{NTF2}_A(z)Q2(z). \end{aligned} \quad (6)$$

Hence, the quantization noise of the first stage, $Q1(z)$, is ideally cancelled leaving only the quantization noise of the second stage, $Q2(z)$; note, however, that $Q2(z)$ is high-order noise shaped by both stages. According to (5), complete cancellation of $Q1(z)$ mandates matching analog signal and noise transfer functions that change with process, voltage, and temperature (PVT) variations to their digital filter equivalents in the NCL that do not. Note from (4) that any mismatches between the analog and digital transfer functions cause leakage to the output of a fraction of $Q1(z)$, typically noise shaped with a lower-order [4], [7].

Complex IF signal digitization and cascade $\Sigma\Delta$ modulation are combined to obtain high-order noise-shaping in a desired bandwidth around a single-sided intermediate frequency. The IF ADC described herein comprises a complex $\Sigma\Delta$ modulator in cascade with a pipeline converter in each of the I and Q paths. An adaptive algorithm simultaneously mitigates mismatches between the I and Q paths, and between ideally identical analog transfer functions in the converter and corresponding digital transfer functions in the NCL. Reduced sensitivity to analog circuit limitations such as I/Q matching and opamp gain is also achieved at the cost of additional digital calibration circuitry. Hence, this approach exploits CMOS technology scaling trends that favor digital circuit implementations, and thus offers a highly integrated digital-intensive solution for receiver design.

Section II reviews basic concepts of complex $\Sigma\Delta$ modulators. Section III describes properties of complex modulators, especially their vulnerability to I/Q mismatches, and key issues related to cascade ADCs are presented in Section IV. The proposed complex $\Sigma\Delta$/pipeline ADC is presented in Section V, and benefits of digital calibration in reducing analog circuit limitations are given in Section VI.

II. Complex Data Converters

The noise and signal spectra of real low-pass and complex bandpass $\Sigma\Delta$ modulators are depicted in Fig. 2. In the low-pass version, the notch of the NTF appears at dc and results in a high signal-to-quantization noise ratio (SQNR) in the frequency band from dc to $+f_b$. In the complex bandpass version, the NTF notch is placed at f_{IF}, which enables high-resolution conversion in the $\sim$2X wider frequency band from $f_{\mathrm{IF}} - f_b$ to $f_{\mathrm{IF}} + f_b$.

Mathematically, the NTF of a low-pass $\Sigma\Delta$ modulator can be transformed to its corresponding complex bandpass version with a notch at $+f_{\mathrm{IF}}$ using the transformation

$$\mathrm{NTF}(z) \rightarrow \mathrm{NTF}(zP^{-1}) \quad (7)$$

where $P = \exp(j2\pi f_{\mathrm{IF}}/f_S)$.

Fig. 3(a) shows a second-order feedforward low-pass modulator where

$$\begin{aligned} I2 &= -z^{-2}Q_n \\ Y &= X + (1 - z^{-1})^2 Q_n \end{aligned} \quad (8)$$

and Fig. 3(b) comprises the corresponding complex bandpass modulator obtained by replacing each real integrator, $H_R(z) = z^{-1}/(1 - z^{-1})$, with its complex counterpart, $H_C(z) = Pz^{-1}/(1 - Pz^{-1})$. This results in the input–output relationship

$$\begin{aligned} Y &= Y_I + jY_Q \\ &= (X_I + jX_Q) + (1 - Pz^{-1})^2(Q_I + jQ_Q) \end{aligned} \quad (9)$$

which has a real signal transfer function $\mathrm{STF} = 1$ and a complex noise transfer function $\mathrm{NTF} = N_r + jN_i = (1 - Pz^{-1})^2$. The digital multipliers normally required for subsequent down-

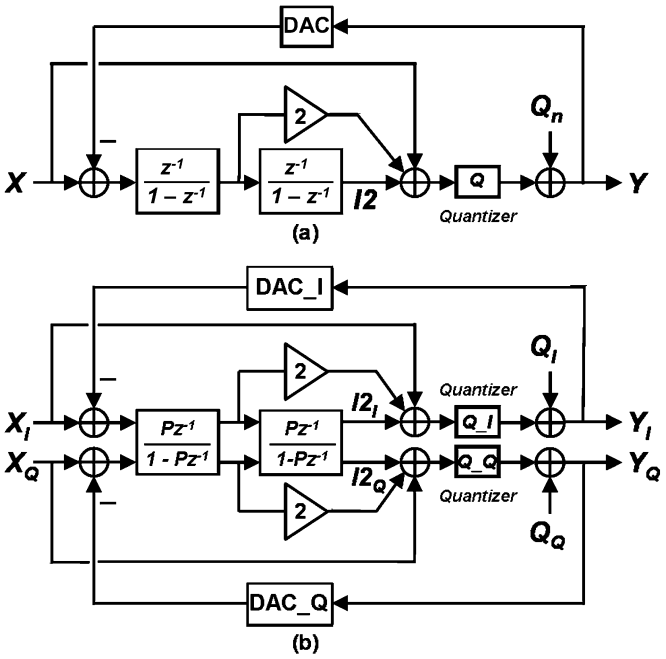

Fig. 3. Feedforward second-order (a) real low-pass and (b) complex bandpass $\Sigma\Delta$ modulators.

conversion may be replaced by AND gates with a proper choice of $f_{\rm IF}$ such that

$$f_{\rm IF} = \left(k \pm \frac{1}{4}\right) \cdot f_s, \qquad k = 0, \pm 1, \pm 2 \ldots \tag{10}$$

With $k = 0$ in (10), $f_{\rm IF} = f_S/4$ and $P = j$. Hence, it follows that $N_r + jN_i = (1 - jz^{-1})^2$ so that

$$\begin{aligned} N_r &= 1 - z^{-2} \\ N_i &= -2z^{-1} \end{aligned} \tag{11}$$

Hence, from (9) with $X_I = X_Q = 0$ and $P = j$

$$\begin{aligned} \mathrm{Y_I + jY_Q} &= (1 - \mathrm{jz}^{-1})^2(\mathrm{Q_I + jQ_Q}) \\ &= (\mathrm{N_r + jN_i})(\mathrm{Q_I + jQ_Q}). \end{aligned} \tag{12}$$

And, therefore

$$\begin{aligned} Y_I &= (N_r Q_I - N_i Q_Q) \\ Y_Q &= (N_r Q_Q + N_i Q_I). \end{aligned} \tag{13}$$

Hence, filtering of the quantization noise, $Q_I + jQ_Q$, by the complex NTF is accomplished using two pairs of *identical* real-valued filters, N_r and N_i, in both the Y_I and Y_Q paths as shown in Fig. 4(a).

III. Properties of Complex Modulators

A. Mathematical Models of Complex $\Sigma\Delta$ Modulators

In a complex bandpass $\Sigma\Delta$ modulator, analog filters are invariably subject to capacitance ratio mismatches, gain and pole frequency errors, etc., so that the N_r and N_i pairs of filters in

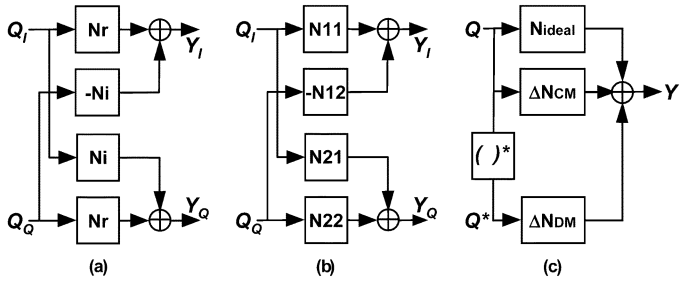

Fig. 4. Equivalent models of complex NTF filtering.

Fig. 4(a) are not matched. In view of these mismatches, the NTF of a practical complex bandpass modulator can be represented by the *four* real-valued filters, $N11, N12, N21$, and $N22$, shown in Fig. 4(b), and the contributions of the quantization noise terms to the outputs may be written as [4]

$$\begin{pmatrix} Y_I \\ Y_Q \end{pmatrix} = \begin{pmatrix} N11 & -N12 \\ N21 & N22 \end{pmatrix} \begin{pmatrix} Q_I \\ Q_Q \end{pmatrix} \tag{14}$$

wherein filter pairs $(N11, N12)$ and $(N21, N22)$ model the I and Q path noise transfer functions, respectively. Clearly, $N11 = N22 = N_r$ and $N12 = N21 = N_i$ in an ideal implementation.

B. CM and DM Mismatches

I/Q mismatches are also analyzed by decomposing them into constituent common-mode (CM) and differential-mode (DM) components using the following definitions:

$$\begin{aligned} \frac{N11 + N22}{2} &= N_{\mathrm{ideal},r} + \Delta N_{\mathrm{CM},r} \\ \frac{N11 - N22}{2} &= \Delta N_{\mathrm{DM},r} \\ \frac{N12 + N21}{2} &= N_{\mathrm{ideal},i} + \Delta N_{\mathrm{CM},i} \\ \frac{N12 - N21}{2} &= \Delta N_{\mathrm{DM},i} \end{aligned} \tag{15}$$

where $N_{\mathrm{ideal},r} = N_r$ and $N_{\mathrm{ideal},i} = N_i$. From (15) it follows that

$$\begin{aligned} N11 &= N_{\mathrm{ideal},r} + \Delta N_{\mathrm{CM},r} + \Delta N_{\mathrm{DM},r} \\ N12 &= N_{\mathrm{ideal},i} + \Delta N_{\mathrm{CM},i} + \Delta N_{\mathrm{DM},i} \\ N21 &= N_{\mathrm{ideal},i} + \Delta N_{\mathrm{CM},i} - \Delta N_{\mathrm{DM},i} \\ N22 &= N_{\mathrm{ideal},r} + \Delta N_{\mathrm{CM},r} - \Delta N_{\mathrm{DM},r}. \end{aligned} \tag{16}$$

Substituting (16) into (14)

$$\begin{aligned} \begin{pmatrix} Y_I \\ Y_Q \end{pmatrix} = &\begin{pmatrix} N_{\mathrm{ideal},r} + \Delta N_{\mathrm{CM},r} & -N_{\mathrm{ideal},i} - \Delta N_{\mathrm{CM},i} \\ N_{\mathrm{ideal},i} + \Delta N_{\mathrm{CM},i} & N_{\mathrm{ideal},r} + \Delta N_{\mathrm{CM},r} \end{pmatrix} \\ &\times \begin{pmatrix} Q_I \\ Q_Q \end{pmatrix} + \begin{pmatrix} \Delta N_{\mathrm{DM},r} & +\Delta N_{\mathrm{DM},i} \\ -\Delta N_{\mathrm{DM},i} & \Delta N_{\mathrm{DM},r} \end{pmatrix} \begin{pmatrix} Q_I \\ -Q_Q \end{pmatrix} \end{aligned} \tag{17}$$

which may be written as

$$Y = N_{\text{ideal}}Q + \Delta N_{\text{CM}}Q + \Delta N_{\text{DM}}Q* \tag{18}$$

where

$$\begin{aligned} N_{\text{ideal}} &= N_{\text{ideal},r} + jN_{\text{ideal},i} \\ \Delta N_{\text{CM}} &= \Delta N_{\text{CM},r} + j\Delta N_{\text{CM},i} \\ \Delta N_{\text{DM}} &= \Delta N_{\text{DM},r} - j\Delta N_{\text{DM},i} \end{aligned} \tag{19}$$

A representation of a complex filter that models such I/Q mismatches is shown in Fig. 4(c). Note that the Y and Q terms in (18) represent frequency-domain quantities. Therefore, for a single tone at image frequency $-f_C$ with $V_n = \exp(-j2\pi f_C t)$, the complex conjugate operation produces a tone at the signal frequency $+f_C$; i.e., $V_n* = \exp(+j2\pi f_C t)$, and vice-versa.

In view of these properties, the effects of CM and DM errors may be interpreted as follows.

- In the ideal case, $\Delta N_{\text{CM}} = \Delta N_{\text{DM}} = 0$ and $\text{NTF} = N_{\text{ideal}} = N_{\text{ideal},r} + jN_{\text{ideal},i}$.
- When $N11$ and $N22$ ($N12$ and $N21$) incur *identical* mismatches from their nominal value, $N_{\text{ideal},r}(N_{\text{ideal},i})$, only CM errors exist; i.e.,

$$\Delta N_{\text{CM}} \neq 0, \quad \Delta N_{\text{DM}} = 0. \tag{20}$$

  In this case, the third term in (18) vanishes, and leakage between the image and signal bands does not occur.
- When $N11$ and $N22$ ($N12$ and $N21$) experience *differential* mismatches such that their average value is $(N11 + N22)/2 = N_{\text{ideal},r}[(N12+N21)/2 = N_{\text{ideal},i}]$, only DM errors exist; i.e.,

$$\Delta N_{\text{CM}} = 0, \quad \Delta N_{\text{DM}} \neq 0. \tag{21}$$

  Because the third term in (18) is nonzero, undesired components from the image band leak into the signal band, and vice-versa.

The above modeling holds for both the noise and signal transfer functions in a complex bandpass $\Sigma\Delta$ ADC. Differential mismatches between the I and Q paths cause nonzero $\Delta\text{NTF}_{\text{DM}}$ and $\Delta\text{STF}_{\text{DM}}$ values. Hence, $\Delta\text{NTF}_{\text{DM}}$ accounts for quantization noise folding from the image band into the signal band, which can seriously degrade SNR. Similarly, a nonzero $\Delta\text{STF}_{\text{DM}}$ causes folding of interferers at the ADC input from the image band into the signal band (Fig. 5); this aliasing can also degrade the SNR of the receiver.

C. Noncommutability of Complex Filters in the Presence of I/Q Mismatches

An important property of complex filtering in the presence of I/Q mismatches is noncommutability. That is, for two I/Q mismatched complex filter blocks A and $B, A \cdot B \neq B \cdot A$. To illustrate this, Fig. 6(a) shows a complex NTF filter bank cascaded with a complex STF filter bank; each is modeled using four real filters to account for possible mismatches. The same filter blocks are cascaded in the opposite order in Fig. 6(b).

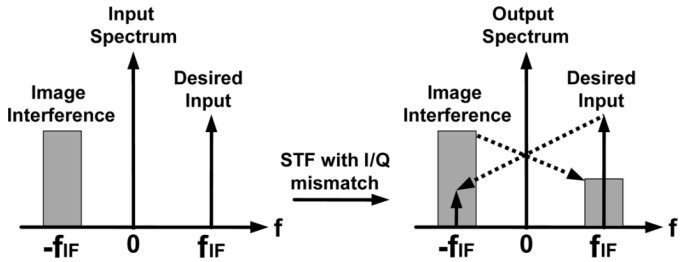

Fig. 5. I/Q mismatch effects on the signal transfer function.

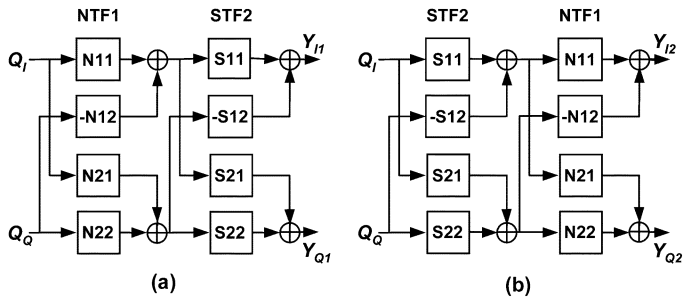

Fig. 6. Two cascaded complex systems with reversed order.

With a complex input, $Q_I + jQ_Q$, the output differences between the two systems are

$$\begin{aligned} \Delta Y_I = Y_{I1} - Y_{I2} &= Q_Q N_{12}(S_{22} - S_{11}) \\ &\quad + Q_Q S_{12}(N_{11} - N_{22}) \\ &\quad + Q_I(S_{21}N_{12} - S_{12}N_{21}) \\ \Delta Y_Q = Y_{Q1} - Y_{Q2} &= Q_I S_{21}(N_{11} - N_{22}) \\ &\quad + Q_I N_{21}(S_{22} - S_{11}) \\ &\quad + Q_Q(S_{12}N_{21} - S_{21}N_{12}). \end{aligned} \tag{22}$$

Equation (22) shows that the two cascaded systems are commutative, $\text{NTF} \cdot \text{STF} = \text{STF} \cdot \text{NTF}$, only when:

- each complex system is perfectly I/Q matched with

$$\begin{aligned} N11 = N22, \quad N12 = N21 \quad \text{and} \\ S11 = S22, \quad S12 = S21 \end{aligned} \tag{23}$$

- or, one of the systems is a real function

$$\begin{aligned} N12 = N21 = 0, \quad N11 = N22 \quad \text{or} \\ S12 = S21 = 0, \quad S11 = S22. \end{aligned} \tag{24}$$

D. Illustration of I/Q Mismatch Effects

Using the analysis above, a second-order complex modulator is simulated to illustrate I/Q mismatch effects. The modulator has the topology shown in Fig. 3(b) with the parameter values given in Table I.

Fig. 7(a) shows the output power spectrum for the ideal modulator of Fig. 3(b) with a -1-dBFS input signal at 41.25 MHz. Only quantization noise is shown; thermal noise is ignored. A deep and sharp notch is observed around f_{IF} =40 MHz. Next, all parameter values are assumed ideal except the I-channel DAC feedback coefficient, $\text{DAC\_}I$ in Fig. 3(b), deviates from its

TABLE I
PARAMETERS OF SECOND-ORDER COMPLEX CONVERTER

Parameter	Value
NTF zero: P	P = j
Sampling Frequency (f_s)	160 MHz
Intermediate Frequency (f_{IF})	40 MHz
Signal Band (f_b)	[30 MHz to 50 MHz]
Image Band (f_{bi})	[-50 MHz to -30 MHz]
Quantizer Resolution (Q_I, Q_Q)	4b
DAC_I, DAC_Q Coefficients	1
Full Scale (V_{FS})	1

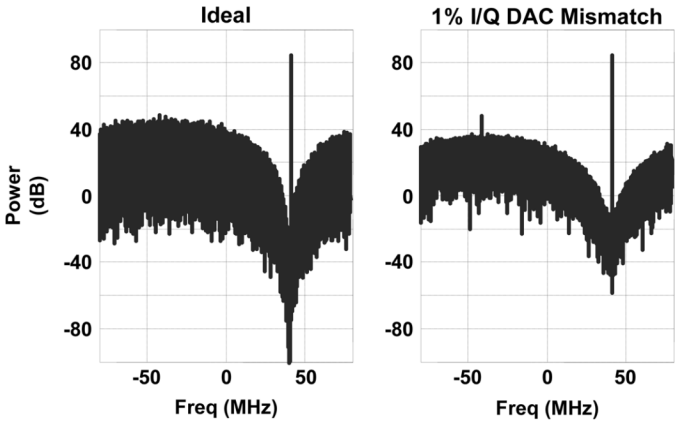

Fig. 7. Output spectra of a second-order complex bandpass ADC [Fig. 3(b)]. (a) Ideal. (b) With a 1% mismatch between the I and Q DACs.

ideal value by 1% due to, for example, a capacitance mismatch. Following the analysis of Section III-B, this imperfection introduces both CM and DM errors into the noise and signal transfer functions. As a result [Fig. 7(b)], quantization noise from the image band is folded into the signal band where it partially fills the notch at $f_{\rm IF}$, and the input signal is reflected into the image band at -41.25 MHz at a significant power level. This image spur does not normally present a serious problem as it can be removed by subsequent complex digital filtering. Similarly, if an interferer is present in the image band at the ADC inputs, it is aliased into the signal band where it corrupts the signal. However, a clean signal can be recovered using a digital signal separator [14].

To gain further insight into the effects of mismatches, the output noise spectrum of Fig. 7(b) is decomposed into its three constituent components according to Fig. 4(c), each filtered by one of three functions: ideal NTF_i, CM error $\Delta\mathrm{NTF}_{\rm CM}$, and DM error $\Delta\mathrm{NTF}_{\rm DM}$. The corresponding power spectra are shown in Fig. 8. Clearly, DM error $\Delta\mathrm{NTF}_{\rm DM}$ is primarily responsible for the increased noise floor because it causes folding of quantization noise into the signal band (30 to 50 MHz) at a relatively high level (<20-dB attenuation).

IV. COMPLEX CASCADE ADCS

The analysis above shows that the performance of complex modulators is sensitive to I/Q mismatches. More specifically, any mismatch between the I and Q paths introduces DM errors in the noise and signal transfer functions, which corrupt the signal in the signal band and degrade ADC SNR performance in two ways.

1) A nonzero $\Delta\mathrm{NTF}_{\rm DM}$ causes folding of image-band quantization noise with little attenuation.
2) A nonzero $\Delta\mathrm{STF}_{\rm DM}$ leads to aliasing of image-band interferers.

Although SNR degradation due to the $\Delta\mathrm{STF}_{\rm DM}$ term can be reduced using a DSP solution [14], quantization noise folding into the signal band presents a serious problem. In this work, the effects of $\Delta\mathrm{NTF}_{\rm DM}$ are mitigated using a complex modulator as the first stage in cascade with pipeline converters as the second stage followed by an adaptive digital NCL block.

A. Cascade $\Sigma\Delta$ Converter

Cascade $\Sigma\Delta$ modulators are widely used because of their attractive stability and high-order noise shaping characteristics. In the two-stage cascade converter of Fig. 1, the first-stage quantization noise, $Q1$, is first filtered by $\mathrm{NTF1}_A$ and then by $\mathrm{STF2}_A$ before being digitized. As shown earlier, the outputs from both stages are combined in the NCL block where $Q1$ is completely cancelled if the digital filters, $\mathrm{NTF1}_D$ and $\mathrm{STF2}_D$, match their analog counterparts, $\mathrm{NTF1}_A$ and $\mathrm{STF2}_A$, respectively.

B. Complex Modulator as First Stage

According to (4), the quantization noise of the first stage $Q1$ is completely cancelled (including the folding of image-band quantization noise into the signal band via the DM error term, $\mathrm{NTF1}_{DM}$), if (5) is satisfied. Three key considerations underpin this approach.

- The commutability property of (24) mandates a real second stage signal transfer function $\mathrm{STF2}_A$, so that $\mathrm{NTF1}_A\mathrm{STF2}_D = \mathrm{STF2}_A\mathrm{NTF1}_D$ with $\mathrm{NTF1}_D = \mathrm{NTF1}_A$ and $\mathrm{STF2}_D = \mathrm{STF2}_A$.
- The digital filters in the NCL should match their analog counterparts. From (4), analog/digital (A/D) filter mismatches cause leakage of Q_1 to the ADC output with low-order noise shaping, which degrades SNR performance.
- From (4), the quantization noise of the second stage $Q2$ is shaped by $\mathrm{NTF2}_A\mathrm{NTF1}_D$. Because $\mathrm{NTF1}_D = \mathrm{NTF1}_A$ is required for the complete cancellation of $Q1, \mathrm{NTF1}_D$ has the same I/Q mismatches as $\mathrm{NTF1}_A$.

C. Considerations for the Second Stage

As shown above, $Q1$ can be cancelled using a real $\mathrm{STF2}_A$ so that only $Q2$ remains in the output. Implementation options for $\mathrm{STF2}_A$ include complex bandpass, real bandpass, and low-pass $\Sigma\Delta$ modulators, or a pipeline converter.

If perfect matching is assumed between the corresponding analog and digital filters ($\mathrm{NTF1}_D = \mathrm{NTF1}_A$) only the second-stage quantization noise remains at the ADC output

$$\begin{aligned} Q_{\rm out}(z) &= Q2(z)\mathrm{NTF2}_A(z)\mathrm{NTF1}_D(z) \\ &= \mathrm{Q2(z)NTF2_A(z)[NTF1_{A\_ideal}(z)} \\ &\quad + \Delta\mathrm{NTF1_{A\_CM}(z)}] \\ &\quad + [\mathrm{Q2(z)NTF2_A(z)}]^*\Delta\mathrm{NTF1_{A\_DM}(z)}. \end{aligned} \tag{25}$$

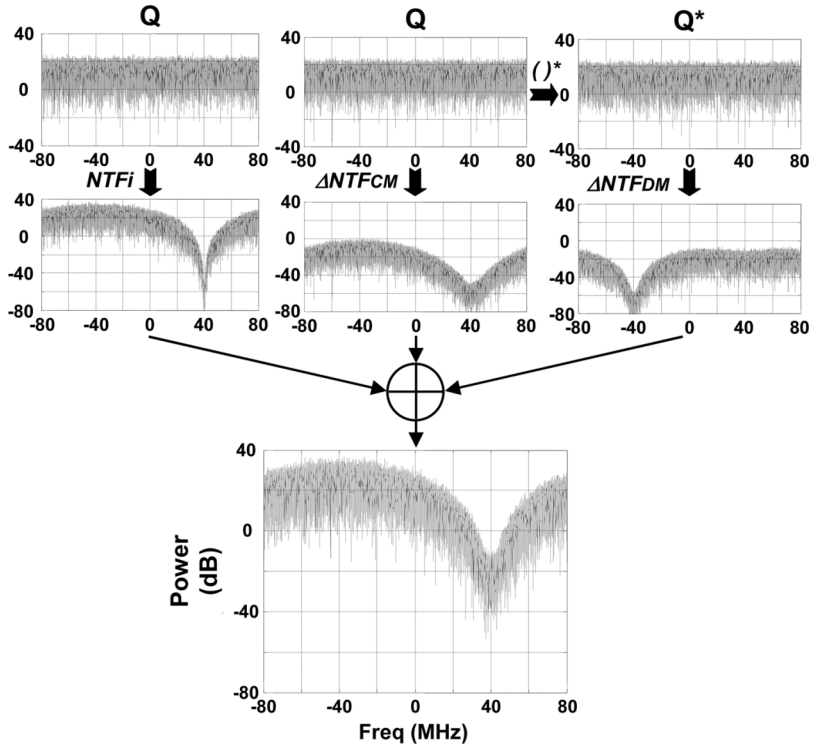

Fig. 8. Constituent quantization noise components of a second-order complex bandpass ADC with a 1% mismatch between the I- and Q-channel DACs.

Recall that the $\Delta\mathrm{NTF1}_{\mathrm{A\_DM}}(z)$ term exhibits minimal attenuation in the signal band, which causes the noise component, $[Q_2(z)\mathrm{NTF2}_A(z)]^*\Delta\mathrm{NTF1}_{A\_\mathrm{DM}}(z)$, to become the dominant noise source for the cascade ADC (Fig. 8). Thus, it is important to choose a second stage with small $Q2$ and an $\mathrm{NTF2}_A$ such that $[Q_2(z)\mathrm{NTF2}_A(z)]^*$ is small in the desired image band.

Fig. 9 compares the noise spectrum $Q_{2\mathrm{out}}(z) = Q_2(z)\mathrm{NTF2}_A(z)$ to its conjugate $Q^*_{2\mathrm{out}}(z) = [Q_2(z)\mathrm{NTF2}_A(z)]^*$, and the noise spectrum after filtering with $\Delta\mathrm{NTF1}_{\mathrm{A\_DM}}(z)$, $Q_{\mathrm{out\_DM}}(z) = Q^*_{2\mathrm{out}}(z)\Delta\mathrm{NTF1}_{\mathrm{A\_DM}}(z)$, for different implementations of the second stage. It is assumed that $\Delta\mathrm{NTF1}_{A\_\mathrm{DM}}(z)$ arises from a 1% mismatch in the I/Q DAC coefficients of the first stage.

As shown in Fig. 9, the quantization noise power, $Q_{2\mathrm{out}}(z)$, is high in the image band, $\mathrm{BW}_I = -30$ to -50 MHz, for both the complex and low-pass modulators because second-order noise shaping creates high quantization noise outside the signal band. This high noise power is folded into the signal band, BW_S =30 to 50 MHz, by the filtering of $\Delta\mathrm{NTF1}_{\mathrm{A\_DM}}(z)$.

For the real bandpass case, the quantization noise is first-order noise shaped in both the signal and image bands so its output noise, $Q_{\mathrm{out\_DM}}(z)$, is low in the signal band compared to the complex and low-pass cases. To achieve high SNR at the ADC output, higher order (> 2) noise shaping is desired in both bands, which raises stability concerns. Higher resolution (> 4b) flash quantizers are also required to decrease $Q2$ at the cost of larger chip area and smaller comparator dc offset voltage margins.

In the case of 9-bit pipeline converters as a second stage, $Q2_{\mathrm{out}}(z)$ has a constant power spectral density (Fig. 9); i.e., no noise shaping occurs. When the small (< -50-dB) white quantization noise is subsequently filtered by $\Delta\mathrm{NTF1}_{\mathrm{A\_DM}}(z)$, the resulting noise density in the signal band is insignificant (< -80 dB) compared to the other approaches.

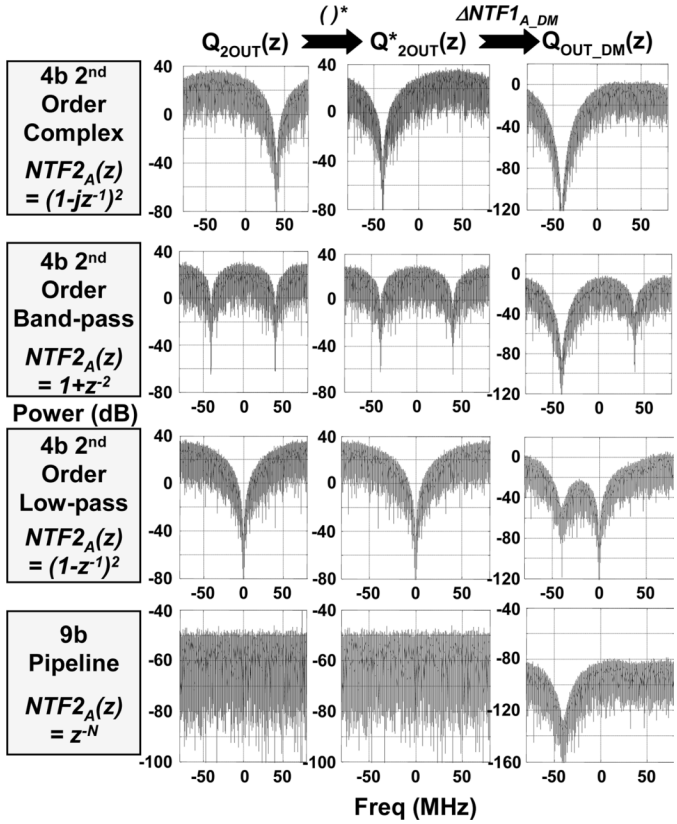

Fig. 9. I/Q mismatch effects on the output quantization noise for different second stages.

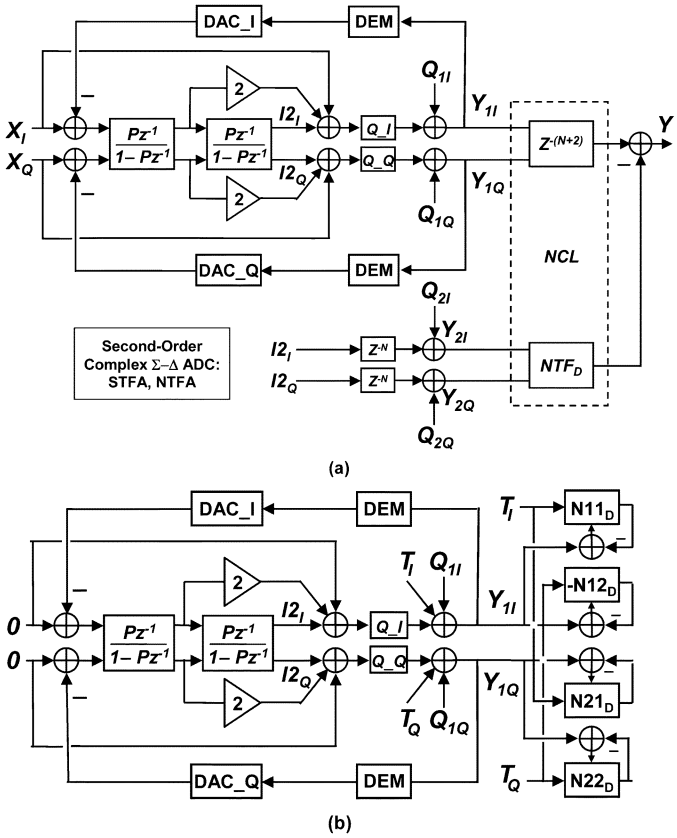

Fig. 10. Block diagram for the complex second-order $\Sigma\Delta$/pipeline converter including noise cancellation logic. (a) Normal operation. (b) Calibration mode.

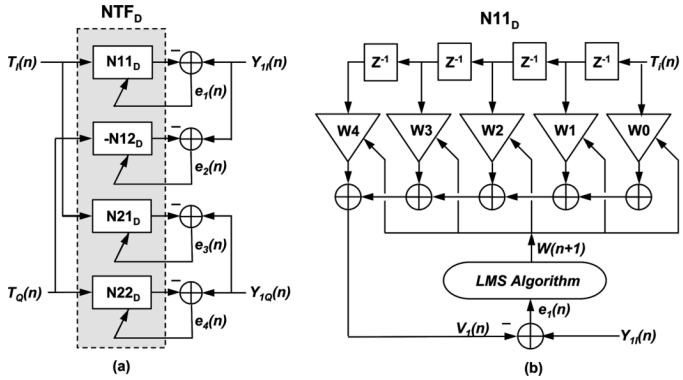

Fig. 11. (a) LMS calibration scheme for the four FIR filters of NTF_D. (b) Details of $N11_D$ filter.

V. Complex $\Sigma\Delta$/Pipeline ADC With Digital Calibration

The results of Section IV show that I/Q mismatch effects in a complex modulator are mitigated by cascading it with a second stage, which has a real STF and small output quantization noise in the image band. Consequently, a pipeline converter is an attractive second-stage implementation. To achieve substantial cancellation of the quantization noise of the first stage, the digital filter $\mathrm{NTF1}_D$ in the NCL is adaptively calibrated to closely approximate its corresponding analog filter $\mathrm{NTF1}_A$.

A. Complex $\Sigma\Delta$/Pipeline Cascade ADC

The complex $\Sigma\Delta$/pipeline cascade ADC is shown in Fig. 10(a); the first stage comprises the second-order complex bandpass $\Sigma\Delta$ modulator described in Section III, and the second stage includes ideally identical pipeline converters in the I and Q paths. To achieve a 12-bit ENOB with a 20-MHz signal bandwidth for wireless local area network (WLAN) applications, the pipeline converters need a resolution of 9b. For complete cancellation of first-stage quantization noise, $Q1$ must be digitized to enable cancellation by the NCL. Consequently, the outputs of the second integrator in the first stage, $I2_I + jI2_Q$, are input to a pair of 9-bit pipeline converters.

The feedforward architecture is chosen for the $\Sigma\Delta$ modulator because of its small signal swing inside the loop and its corresponding low distortion [17]. Another advantage of the feedforward topology as mentioned above is that its quantization noise is output directly as

$$I2_I + jI2_Q = z^{-2}(Q1_I + jQ1_Q). \tag{26}$$

Thus, the DACs that are otherwise required for explicit $Q1$ extraction with other topologies are not needed.

The complex digital outputs from the first and second stages, Y_1 and Y_2, respectively, are input to the NCL block. Ideally with $\mathrm{NTF}_D = \mathrm{NTF1}_A = \mathrm{NTF}_A = (1 - jz^{-1})^2$, $Q1$ is completely cancelled in the overall output

$$\begin{aligned} Y &= X \cdot \mathrm{STF}_A \cdot z^{-(N+2)} \\ &\quad + Q1 \cdot (\mathrm{NTF}_A - \mathrm{NTF}_D) \\ &\quad \cdot z^{-(N+2)} - Q2 \cdot \mathrm{NTF}_D \\ &= X \cdot \mathrm{STF}_A \cdot z^{-(N+2)} - Q2 \cdot \mathrm{NTF}_D \end{aligned} \tag{27}$$

where $X, Y, Q1$, and $Q2$ are complex signals.

In practice, because of analog imperfections such as integrator gain and pole errors introduced by finite opamp dc gain, capacitor mismatches, PVT variations, etc., NTF_A deviates from ideal, which creates mismatches with NTF_D. Consequently, quantization noise of the first stage, $Q1$, leaks to the output with a low-order noise shaping of $\mathrm{NTF}_A - \mathrm{NTF}_D$ where it degrades the SNR performance of the ADC.

To achieve cancellation of $Q1$, the digital filter NTF_D is adaptively calibrated so that its frequency response closely matches that of the real analog filter NTF_A.

B. LMS Calibration for the Complex $\Sigma\Delta$/Pipeline ADC

During calibration, the ADC input signal is set to zero. Two uncorrelated pseudo-random sequences, T_I and T_Q, are generated using linear feedback shift registers, and injected into the I and Q paths, respectively, to facilitate adaptive digital calibration [18]. Specifically, they are injected as shown in Fig. 10(b) so that they experience the same transfer function as the quantization noise of the first stage.

Because of the complex nature of NTF_A (Fig. 4), the equivalent digital filter NTF_D is implemented using four real finite-impulse response (FIR) filters, $N11_D, N12_D, N21_D$, and $N22_D$ [Figs. 10(b), 11(a)]. The least-mean-square (LMS) adaptation algorithm is chosen for its simplicity and stability to simultaneously calibrate the four FIR filters [Fig. 11(b)] [19].

T_I and T_Q are also input to the corresponding digital FIR filters. Their outputs are compared to the corresponding analog filter outputs, and the resulting error signals,

TABLE II
DIGITAL FILTER COEFFICIENTS

FIR	NTFA	NTFD w/o calibration [W0…W4]	NTFD with calibration [W0, …, W4]
N11	[1, 0, -1.01, 0, 0.0101]	[1, 0, -1, 0, 0]	[0.997, 0.002, -1.009, -0.002, 0.013]
N21	[0, 2, 0, 0.02, 0.0002]	[0, 2, 0, 0, 0]	[0.002, -2.004, 0.002, 0.018, 0.003]
N12	[0, -2.02, 0, 0.0202, 0]	[0, -2, 0, 0, 0]	[0, -2.016, -0.002, 0.023, 0.004]
N22	[1, 0, -1.04, 0, 0.0004]	[1, 0, -1, 0, 0]	[1.002, 0, -1.042, 0, -0.004]

$e_k(n), k = 1,2,3,4$ [Figs. 10(b), 11(a)] are used to adapt the filter coefficients with a step size of μ,

$$W_k(n+1) = W_k(n) + 2 \cdot \mu \cdot e_k(n) \cdot T_{I/Q}(n) \tag{28}$$

such that the mean square value of $e_k(n)$ is minimum

$$\frac{\partial \left(E[e_k^2(n)]\right)}{\partial W_k(n)} = 0, \qquad \text{for } k = 1,2,3,4. \tag{29}$$

Fig. 11(b) shows calibration details for one of the four digital FIR filters, $N11_D$. With an input signal, $T_I(n)$, the filter output, $V_1(n)$, is compared to the real part of first-stage output, $Y_{1I}(n)$. The FIR filter coefficient vector, $W(n)$, is adjusted until convergence to the optimum value is achieved (Φ is the cross-correlation function)

$$W(z) = \frac{\Phi_{Y_{1I}T_I}(z)}{\Phi_{T_IT_I}(z)}. \tag{30}$$

As $Y_{1I} = N11_A(T_I + Q_I) - N12_A(T_Q + Q_Q)$ and assuming that $T_I, T_Q, Q1_I$ *and* $Q1_Q$ are uncorrelated stationary signals with $E[T_I] = E[T_Q] = 0$, (30) simplifies to

$$\begin{aligned} W(z) &= \frac{\Phi_{Y_{1I}T_I}(z)}{\Phi_{T_IT_I}(z)} \\ &= \frac{N11_A(z) \cdot \Phi_{T_IT_I}(z)}{\Phi_{T_IT_I}(z)} \\ &= N11_A(z). \end{aligned} \tag{31}$$

Thus, after calibration the frequency response of $N11_D$ closely approximates that of its analog counterpart $N11_A$.

In Table II, the real analog filter coefficients (determined using *Maple*) of NTFA in the presence of 1% I/Q DAC mismatches are compared to the coefficients of the digital filter NTF_D with and without calibration. The calibrated digital coefficients after 2^{22} iterations (an operating duration of 26.2 ms at $f_s = 160$ MHz) with a calibration step size of 2^{-11} closely match those assumed for the analog filter including I/Q mismatch. The calibration signals, T_I and T_Q, are 32-bit pseudorandom zero-mean binary signals with discrete levels of $\pm$LSB.

C. Simulation Results

To verify that the sensitivity of the complex ADC to I/Q mismatches is significantly reduced using the calibrated complex $\Sigma\Delta$/pipeline architecture, the cascaded converter [Fig. 10(a)] is simulated with and without I/Q mismatches.

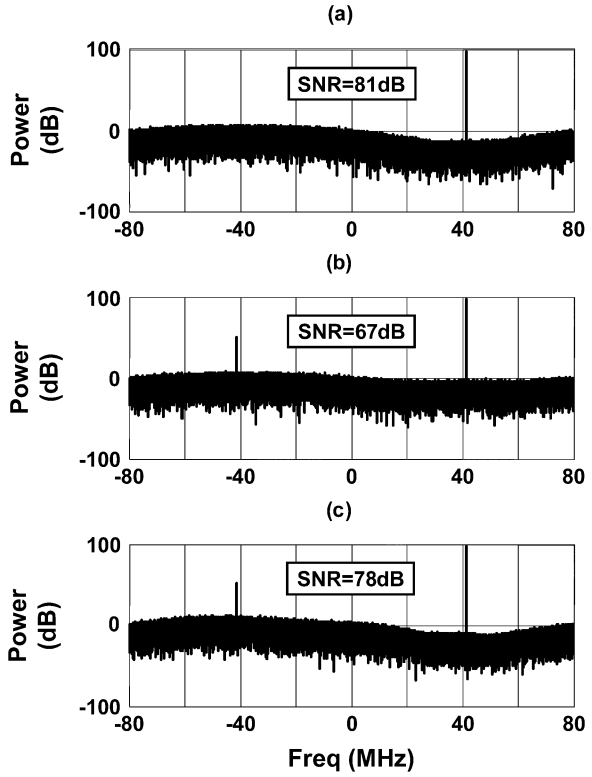

Fig. 12. Output spectra for the complex $\Sigma\Delta$/pipeline ADC. f_s =160 MHz, f_{IF} = 40 MHz, BW =20 MHz. (a) Ideal. (b) $\mathrm{NTF_A}$ 1% DAC I/Q mismatch w/o calibration. (c) $\mathrm{NTF_A}$1% DAC I/Q mismatch with calibration.

In the ideal case, the first-stage complex $\Sigma\Delta$ modulator has perfect I/Q matching and the digital filter NTF_D matches its corresponding analog filter. Consequently, the first-stage quantization noise, $Q1$, is completely cancelled and what remains at the overall ADC output is thermal noise and $Q2$ noise-shaped with $\mathrm{NTF}_D = (1 - jz^{-1})^2$. The output spectrum of the ideal ADC [Fig. 12(a)] exhibits an SNR of 81 dB over a 20-MHz bandwidth with a sampling frequency of 160 MHz.

With a 1% DAC feedback coefficient mismatch between the complex $\Sigma\Delta$ modulator I and Q channels, the digital filter no longer matches its analog counterpart, which causes $Q1$ leakage to the ADC output with a low-order filtering of $(\mathrm{NTF}_A - \mathrm{NTF}_D)$. As shown in Fig. 12(b), this $Q1$ leakage causes the SNR of the ADC to decrease by a significant amount—14 dB.

To realize nearly complete cancellation of the quantization noise in the first stage, the digital filter coefficients of NTF_D are adaptively calibrated to closely match the I/Q-mismatched analog filter NTF_A. Fig. 12(c) shows the ADC output spectrum after calibration; the SNR of the converter is restored to 78 dB—only 3 dB less than ideal. The loss in SNR occurs because the quantization noise of the second stage is now filtered by the I/Q-mismatched NTF_D. Using a pair of 9-bit pipeline converters as the second stage of the ADC, $Q2$ is relatively small and the complex $\Sigma\Delta I/Q$ mismatch effects are greatly reduced. Although only DAC I/Q mismatch is considered here, the approach is able to calibrate out any I/Q mismatch in the complex

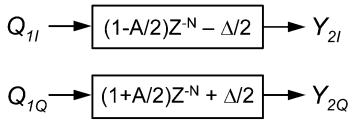

Fig. 13. Non-ideal second-stage pipeline ADC pair.

modulator and mitigate its effect by nearly complete cancellation of the first-stage quantization noise.

The improved performance of the ADC comes at the cost of additional hardware and power consumption associated with the LMS digital calibration circuitry. However, calibration is performed off-line so that much of the digital noise cancellation logic can also be used during calibration. Simulations show that optimum resolution/power dissipation is realized using five 14-bit FIR filter taps as shown in Fig. 11(b). Although the NCL adds dynamic power consumption, both die area and power reduce dramatically with CMOS technology scaling. Consequently, this mixed-signal approach is scaling friendly.

VI. Analog Design Requirements

As shown in previous sections, the complex ADC I/Q mismatch effects are mitigated by cascading the complex $\Sigma\Delta$ modulator with a pair of 9-bit pipeline converters and cancelling the first-stage quantization noise using digital noise cancellation logic. For complete cancellation, the complex ADC is adaptively calibrated so that the digital filters match their analog counterparts. In addition to reduced I/Q matching requirements, other analog design requirements are also relaxed to enable higher speed and lower power designs.

A. Pipeline Converter Non-Ideality

So far, the pipeline converter I/Q pair used in the second stage is assumed to be perfectly matched to its digital counterpart, z^{-N}. In practice, of course, there are always nonidealities that cause mismatches between the I/Q channels, analog and digital filters, etc. Gain and dc offset errors are two important nonidealities of the pipeline converters. To determine the effects of their nonidealities on the cascade complex ADC, the second-stage analog pipeline pair is modeled with both gain error, A, and dc offset error, Δ, as depicted in Fig. 13.

Fig. 14 compares the output spectra of the complex $\Sigma\Delta$/pipeline ADC with nonzero pipeline gain and dc offset errors to the ideal case. With a gain error of 10%, the SNR of the ADC is decreased by only 2 dB. A 5% dc offset introduces a tone at dc but maintains the same SNR performance over the signal band. Compared to the first-stage nonidealities, which are always the critical limiting factors for the overall system performance, the second-stage pipeline converter gain and dc offset errors have small effects, which relaxes the pipeline converter design requirements.

B. Opamp Finite dc Gain

Using digital calibration, the first-stage complex filter is effectively desensitized to opamp dc gain variations. A pair of

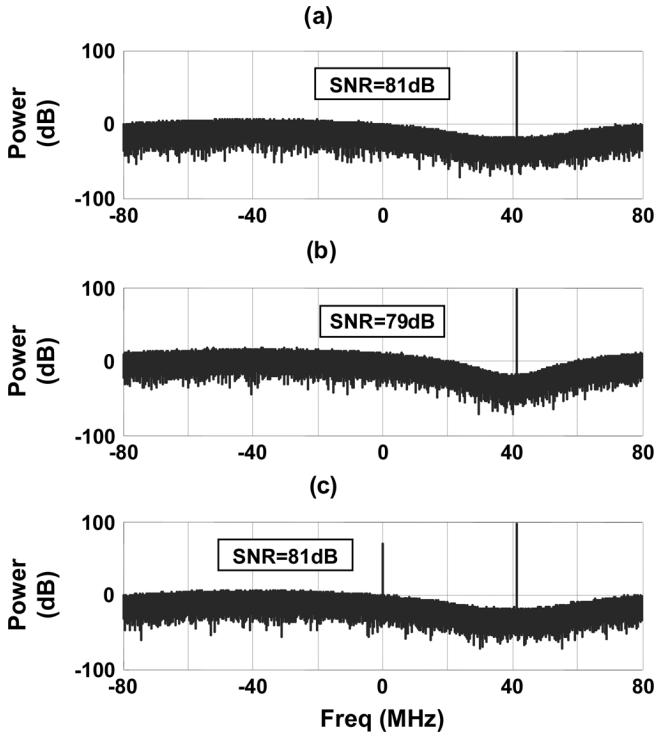

Fig. 14. Output spectra with pipeline nonidealities. $f_s = 160$ MHz, $f_{\rm IF} = 40$ MHz, BW $= 20$ MHz. (a) Ideal (b) 10% pipeline gain error. (c) 5% pipeline dc offset.

cross-coupled real integrators comprises a complex integrator [Fig. 15(a)] [13] where $H(z) = Pz^{-1}/(1 - Pz^{-1})$, and

$$P = \exp\left(j\frac{2\pi f_{\rm IF}}{f_S}\right) = (1+d) + jc. \tag{32}$$

Ideally, each real integrator $z^{-1}/(1-z^{-1})$ is implemented using an opamp with infinite dc gain. In practice, finite opamp dc gain introduces a gain error, $(1 - \varepsilon_g)$, and a pole frequency error, $(1 - \varepsilon_p)$, to a real integrator [Fig. 15(b)]. Those errors, in turn, cause gain and pole frequency errors in the complex integrator according to

$$H(z) = \frac{(1-\varepsilon_g)Pz^{-1}}{1-(P-\Delta P)z^{-1}}$$
$$\Delta P = \varepsilon_p + \mathrm{d}\varepsilon_g + \mathrm{jc}\varepsilon_g. \tag{33}$$

The gain/pole errors thus introduce mismatches between the analog and digital filters, which lead to incomplete cancellation of the first-stage quantization noise. Fig. 16(a) shows the output spectra of a complex $\Sigma\Delta$/pipeline ADC where the real integrators in the complex $\Sigma\Delta$ modulator are implemented using opamps with dc gains of 35 dB. The A/D filter mismatches cause first-stage quantization leakage to the output, which degrades the SNR of the ADC from its ideal value of 81 to 75 dB. After digital calibration, the SNR is improved to 79.6 dB [Fig. 16(b)]. However, there remains a 1.4-dB loss in SNR due to the low opamp gain. As is common practice, opamps with high dc gain ($>$ 60 dB) are used in the real integrators so that the corresponding analog filters closely match their digital counterparts

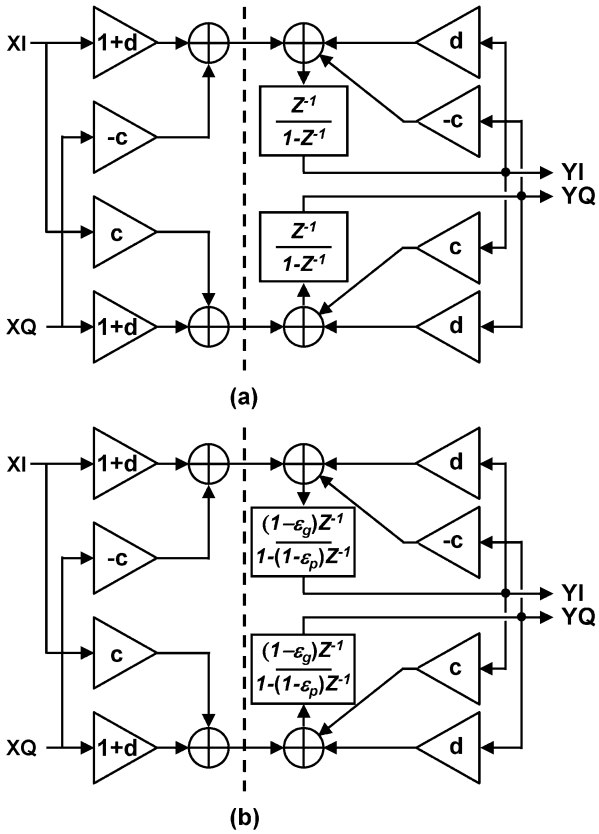

Fig. 15. Complex integrator with (a) infinite, and (b) finite opamp gain. (Note: $\mathrm{P} = \mathrm{j}$ requires $\mathrm{c} = 1$ and $\mathrm{d} = -1$).

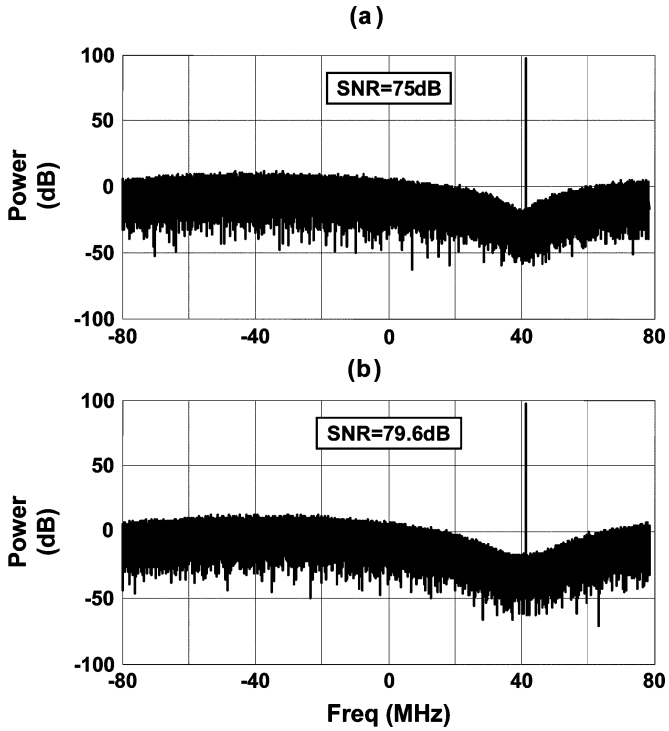

Fig. 16. Output spectra for the complex $\Sigma\Delta$/pipeline ADC using low-gain opamps. f_s =160 MHz, f_{IF} = 40 MHz, BW =20 MHz. (a) 35-dB gain without calibration. (b) 35-dB gain with calibration.

to achieve maximum SNR. Of course, high gain comes at the cost of power, speed and voltage headroom.

It has been demonstrated that digital calibration reduces opamp dc gain errors, and applies well to other analog imperfections such as capacitance mismatches, PVT variations, etc. Both the CM and DM errors introduced by those imperfections can be calibrated out via the four FIR digital filters of Fig. 11(a).

VII. Conclusion

Complex converters can digitize analog signals at intermediate frequencies with excellent bandwidth/power efficiency, which makes them good candidates for digital receivers; but, they are vulnerable to I/Q mismatches. An I/Q mismatch not only causes aliasing of image-band interferers into the signal band, quantization noise in the image band is also reflected into the signal band as a result of the DM error. Although the corrupted signal can be recovered from the image interference using a digital signal separator, the folded quantization noise can seriously degrade SNR performance. This paper presents a solution to mitigate I/Q mismatch effects in a complex $\Sigma\Delta$ ADC that introduces a complex $\Sigma\Delta$/pipeline ADC architecture along with digital calibration. With a 9-bit pipeline pair as a second converter stage and noise cancellation logic, the quantization noise of the first stage is ideally completely cancelled, including leakage to the output owing to the CM and DM errors. Even in the presence of a 1% mismatch in the I/Q DAC coefficients of the first stage, the complex $\Sigma\Delta$/pipeline ADC achieves a simulated SNR of 78 dB after calibration.

Through the use of an adaptive digital calibration algorithm, the digital filter is closely matched to its analog counterpart, and, thus, analog design requirements of the ADC are relaxed. The second-stage pipeline converter requirements, for example, are relaxed with respect to gain errors, dc offsets, etc.

The proposed architecture exploits the high-speed DSP advocated by CMOS scaling so that the complex converter design is digital intensive and scaling friendly.

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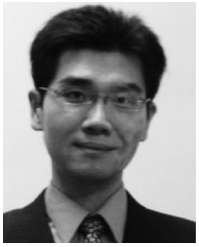
Ms. Tang was a recipient of the Analog Devices Outstanding Student Designer Award in 2006.



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Dr. Allstot has received several outstanding teaching and advising awards. Other awards include the 1978 IEEE W.R.G. Baker Prize Paper Award, 1995 IEEE Circuits and Systems Society (CAS-S) Darlington Award, 1998 IEEE Int. Solid-State Circuits Conf. (ISSCC) Beatrice Winner Award, 1999 IEEE CAS-S Golden Jubilee Medal, 2004 Technical Achievement Award of the IEEE CAS-S, the 2005 Aristotle Award of the Semiconductor Research Corp, and the 2008 University Research Award of the Semiconductor Industries Association. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1990 to 1993 and the Editor-in-Chief from 1993 to 1995. He was on the Technical Program Committee, IEEE Custom Integrated Circuits Conference, from 1990 to 1993, Education Award Committee, IEEE CAS-S, from 1990 to 1993, Board of Governors, IEEE CAS-S, from 1992 to 1995, Technical Program Committee, IEEE International Symposium on Low-Power Electronics and Design, from 1994 to 1997, Mac Van Valkenberg Award Committee, IEEE CAS-S, from 1994 to 1996, and Technical Program Committee, IEEE ISSCC, from 1994 to 2004. He was the 1995 Special Sessions Chair, IEEE International Symposium on CAS (ISCAS), an Executive Committee Member and the Short Course Chair, ISSCC, from 1996 to 2000, Co-Chair, IEEE Solid-State Circuits (SSC) and Technology Committee, from 1996 to 1998, Distinguished Lecturer, IEEE CAS-S, from 2000 to 2001, Distinguished Lecturer, IEEE SSC Society, from 2006 to 2007, the Co-General Chair, IEEE ISCAS in 2002 and in 2008, and President-Elect, IEEE CAS-S, 2008.