Floating Point Puzzles

For each of the following C expressions, either:
- Argue that it is true for all argument values
- Explain why not true

1. $x \equiv (\text{int})(\text{double}) \times$ T
2. $x \equiv (\text{int})(\text{float}) \times$ F
3. $f \equiv (\text{float})(\text{double}) \times$ T
4. $d \equiv (\text{double})(\text{float}) \times$ F
5. $f \equiv -(-f);$ T
6. $1.0/2 \equiv 1/2.0$ T
7. $d \times d \geq 0.0$ T
8. $(f+d)-f \equiv d$ F

int $x = \ldots$;
float $f = \ldots$
double $d = \ldots$

Assume neither $d$ nor $f$ is NaN
Summary

- IEEE Floating Point has clear mathematical properties
- Represents numbers of form $M \times 2^E$
- One can reason about operations independent of implementation
  - As if computed with perfect precision and then rounded
- Not the same as real arithmetic
  - Violates associativity/distributivity
  - Makes life difficult for compilers & serious numerical applications programmers
## Intel x86 Evolution: Milestones

<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
<th>MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>8086</td>
<td>1978</td>
<td>29K</td>
<td>5-10</td>
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<tr>
<td>386</td>
<td>1985</td>
<td>275K</td>
<td>16-33</td>
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<tr>
<td>Pentium 4F</td>
<td>2005</td>
<td>230M</td>
<td>2800-3800</td>
</tr>
</tbody>
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- First 16-bit processor. Basis for IBM PC & DOS
- 1MB address space
- First 32 bit processor, referred to as IA32
- Added “flat addressing”
- Capable of running Unix
- 32-bit Linux/gcc uses no instructions introduced in later models
- First 64-bit processor
- Meanwhile, Pentium 4s (Netburst arch.) phased out in favor of “Core” line
Intel x86 Processors

• Machine Evolution
  – 486      1989      1.9M
  – Pentium  1993      3.1M
  – Pentium/MMX 1997     4.5M
  – PentiumPro 1995     6.5M
  – Pentium III 1999    8.2M
  – Pentium 4  2001     42M
  – Core 2 Duo 2006    291M

• Added Features
  – Instructions to support multimedia operations
    • Parallel operations on 1, 2, and 4-byte data, both integer & FP
  – Instructions to enable more efficient conditional operations

• Linux/GCC Evolution
  – Very limited
<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
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<tbody>
<tr>
<td>Itanium</td>
<td>2001</td>
<td>10M</td>
</tr>
<tr>
<td></td>
<td>• First shot at 64-bit architecture: first called IA64</td>
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</tr>
<tr>
<td></td>
<td>• Radically new instruction set designed for high performance</td>
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<td></td>
<td>• Can run existing IA32 programs</td>
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<td></td>
<td>• On-board “x86 engine”</td>
<td></td>
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<tr>
<td></td>
<td>• Joint project with Hewlett-Packard</td>
<td></td>
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<tr>
<td>Itanium 2</td>
<td>2002</td>
<td>221M</td>
</tr>
<tr>
<td></td>
<td>• Big performance boost</td>
<td></td>
</tr>
<tr>
<td>Itanium 2 Dual-Core</td>
<td>2006</td>
<td>1.7B</td>
</tr>
<tr>
<td>Itanium has not taken off in marketplace</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>• Lack of backward compatibility, no good compiler support, Pentium 4 got too good</td>
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</tbody>
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x86 Clones: Advanced Micro Devices (AMD)

• Historically
  – AMD has followed just behind Intel
  – A little bit slower, a lot cheaper

• Then
  – Recruited top circuit designers from Digital Equipment Corp. and other downward trending companies
  – Built Opteron: tough competitor to Pentium 4
  – Developed x86-64, their own extension to 64 bits

• Recently
  – Intel much quicker with dual core design
  – Intel currently far ahead in performance
  – em64t backwards compatible to x86-64
Intel’s 64 bit

• Intel Attempted Radical Shift from IA32 to IA64
  – Totally different architecture (Itanium)
  – Executes IA32 code only as legacy
  – Performance disappointing
• AMD Stepped in with Evolutionary Solution
  – x86-64 (now called “AMD64”)
• Intel Felt Obligated to Focus on IA64
  – Hard to admit mistake or that AMD is better
• 2004: Intel Announces EM64T extension to IA32
  – Extended Memory 64-bit Technology
  – Almost identical to x86-64!
• **Architecture**: (also instruction set architecture: ISA) The parts of a processor design that one needs to understand to write assembly code.

• **Microarchitecture**: Implementation of the architecture.

• **Architecture examples**: instruction set specification, registers.

• **Microarchitecture examples**: cache sizes and core frequency.
Assembly Programmer’s View

• Programmer-Visible State
  – PC: Program counter
    • Address of next instruction
    • Called “EIP” (IA32) or “RIP” (x86-64)
  – Register file
    • Heavily used program data
  – Condition codes
    • Store status information about most recent arithmetic operation
    • Used for conditional branching

– Memory
  • Byte addressable array
  • Code, user data, (some) OS data
  • Includes stack used to support procedures
Turning C into Object Code

– Code in files `p1.c` `p2.c`
– Compile with command: `gcc -O p1.c p2.c -o p`
  • Use optimizations (`-O`)
  • Put resulting binary in file `p`

```
text
  C program (`p1.c` `p2.c`)

  Compiler (`gcc -S`)
  Assembler (`gcc` or `as`)
```

```
text
  Asm program (`p1.s` `p2.s`)

  Assembler (`gcc` or `as`)
```

```
binary
  Object program (`p1.o` `p2.o`)

  Linker (`gcc` or `ld`)
```

```
binary
  Executable program (`p`)
```

Static libraries (`.a`)