• For Friday: 334 – 364

• Bomb lab?
int Sum(int *Start, int Count) {
    int sum = 0;
    while (Count) {
        sum += *Start;
        Start++;
        Count--;
    }
    return sum;
}

Compare to 4.6, p346
Circuits and HCL

- HCL: Hardware Control Language
  - Describes control logic in processor designs

```cpp
bool eq = (a && b) ++ (!a && !b);
354, fig 4.10
```

```cpp
bool Eq = (A == B);
356, fig 4.12
```

```cpp
bool out = (s && a) ++ (!s && b);
355, fig 4.11
```
ALU: Arithmetic Logic Unit

• Four-way mux:

  int Out4 = [
    : A;
    : B;
    : C;
    : D;
  ];
ALU: Arithmetic Logic Unit

• **Four-way mux:**

```c
int Out4 = [
    !s1 && !s0      : A; #00
    !s1             : B; #01
    !s0             : C; #10
    1                : D; #11
];
```
ALU: Arithmetic Logic Unit

- Four-way mux:

  int Out4 = [
    !s1 && !s0 : A; #00
    !s1 : B; #01
    !s0 : C; #10
    1 : D; #11
  ];

- ALU

  0: +
  1: -
  2: &
  3: ^
Where do Gates Come From?

- Mechanical: Charles Babbage, Analytical Engine
- Vacuum Tubes
Transistors

- $V_{RC} = I_{CE} \times R_C$, the voltage across the load (the lamp with resistance $R_C$)
- $V_{RC} + V_{CE} = V_{CC}$, the supply voltage shown as 6V
Simple Memory

• Cross-coupled NOR gates
  – S-R latch (set, reset latch)
  – Unclocked
  – S = 1 means Q should be 1
  – R = 1 means !Q should be 1
  – S = 1 && R=1?

• D flip-flop (also a D latch)
  – Inputs: data value, D, clock signal, C
  – Outputs: Q, and !Q
  – C = 1 means open, C=0 means closed
Registers: Sequential Circuits

• Combinational Circuit: No internal storage

• Input, State, Output
  – State and output changed on rising edge

• Register File (p. 362)
  – Read ports: srcA/valA, srcB/valB
  – Write port: valW + dstW
  – Clock
  – “val” and “dst” are registers: {0-7, F}
  – Race conditions
Random-Access Memory

- Input: read or write? write
- Input: Address, data in
- Output: data out
- Clock
- Error flag